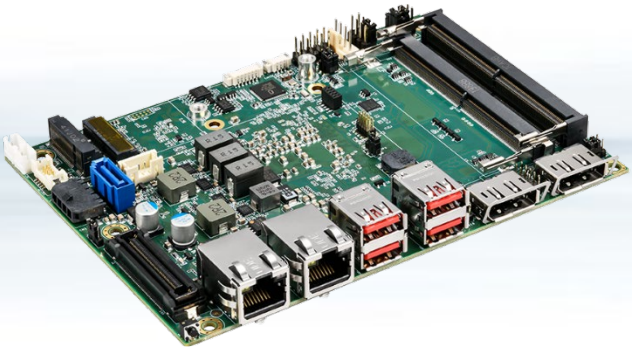
USER GUIDE



3.5"-SBC-RPL

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3.5"-SBC-RPL - USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author/ Editor
1.0	Initial Issue	2025-Mar-28	YS

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol informs of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

This user guide describes the 3.5"-SBC-RPL board made by Kontron. This board will also be denoted 3.5"-SBC-RPL within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the 3.5"-SBC-RPL board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can be downloaded from Kontron's Web Page.

2/ Installation Procedures

2.1. Installing the Board

NOTICE

ESD Sensitive Device!

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure the DC single supply used is within the range between 9 V and 36 V with suitable cable kit and PS-ON# active.

NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

2. **Insert the DDR5 5200 module**
   Be careful to push the memory module in the slot before locking the tabs.
3. **Connecting interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.
4. **Connect and turn on PSU**
   Connect PSU to the board by the 3.0 mm pitch 1x4-pin wafer connector.
5. **BIOS setup**
   Enter the BIOS setup by pressing the <DEL> key during boot up.
   Enter "Exit Menu" and Load Setup Defaults.

To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

6. **Mounting the board in chassis**

NOTICE

When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2. Chassis Safety Standards

Before installing the 3.5"-SBC-RPL in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

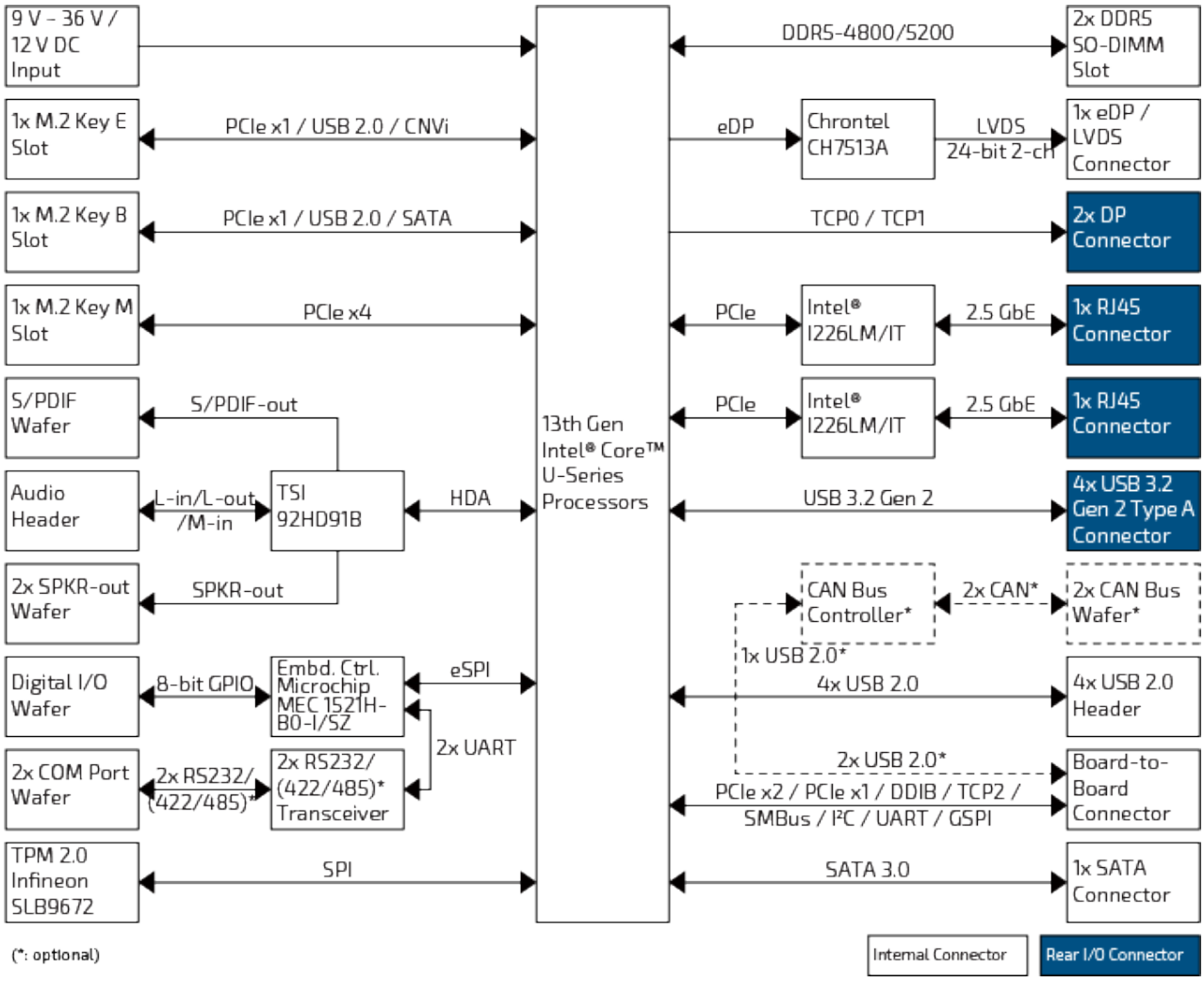
VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

3/ System Specifications

3.1. System Block Diagram

Figure 1: System Block Diagram 3.5"-SBC-RPL



3.2. Component Main Data

The table below summarizes the features of the 3.5"-SBC-RPL single board computer.

Table 1: Component Main Data

System	
Processor	▶ 13th Gen Intel® Core™ U-Series Processors ▶ Intel® U300E
Memory	▶ 2x DDR5 SO-DIMM
Video	
Display Interface	▶ 1x eDP / LVDS (4096 x 2304 @ 120 Hz / 24-bit, 2-ch, 1920 x 1200 @ 60 Hz) ▶ 2x DP (7680 x 4320 @ 60 Hz, Full-size DP on rear)
Multiple Display	▶ Quadruple (more display I/Os supported via board-to-board connector)
Audio	
Audio Codec	▶ TSI 92HD91B
Audio Display	▶ 1x Speaker-out (Stereo, 3 W, by header) ▶ 1x Line-in (by header) ▶ 1x Line-out (by header) ▶ 1x Mic-in (by header) ▶ 1x S/PDIF Out (by header)
Network Connection	
Ethernet	▶ 2x 2.5 GbE LAN (RJ45 on rear, Intel® I226-LM/IT) ▶ TSN support (variants with Core™ URE Series CPUs)
Peripheral Connection	
USB	▶ 4x USB 3.2 Gen 2 (Type A on rear) ▶ 4x USB 2.0 (by header, -1 in case of 2x CAN Bus, -2 in case of 2x USB 2.0 in B2B)
Serial Port	▶ 2x RS232 (def.) / RS232/422/485 (opt.) (by header, Tx/Rx only in RS232 signal)
Other I/Os	▶ 4x DI (by header) ▶ 4x DO (by header) ▶ 2x CAN Bus (optional, by header, trade off 1x USB 2.0 header)
Storage & Expansion	
SATA	▶ 1x SATA 3.0
M.2	▶ 1x M.2 Key B (Type 2242 / 3042 / 3052 / 2280, w/ PCIe x1 / USB 2.0 / SATA / UIM) ▶ 1x M.2 Key E (Type 2230, w/ PCIe x1 / USB 2.0 / CNVi) ▶ 1x M.2 Key M (Type 2280, w/ PCIe x4)
SIM Card Holder	▶ 1x SIM Card Holder (by header)
Extended Board-to-board Connector	▶ 1x DDI ▶ 1x TCP ▶ 1x PCIe x2 ▶ 1x PCIe x1 ▶ 1x SM Bus

System	
	▶ 1x I^2C ▶ 1x UART ▶ 1x GSPI ▶ 2x USB 2.0 (optional, replacing the route to 2x internal USB 2.0)
Power	
Input Voltage	▶ DC 9 V ~ 36 V (Configuration 1) ▶ DC 12 V (Configuration 2)
Connector	▶ 1x4-pin pitch 3.0 mm Wafer
Firmware	
BIOS	▶ AMI uEFI BIOS w/ 256 Mb SPI Flash
Watchdog	▶ Programmable WDT to generate system reset event
H/W Monitor	▶ Voltages ▶ Temperatures
Real Time Clock	▶ Processor integrated RTC
Security	▶ TPM 2.0 (Infineon SLB 9672)
System Control & Monitoring	
Button, Switch & Indicator	▶ 1x Power Button (on rear) ▶ 1x Power LED (Green, on rear) ▶ 1x Standby LED (Yellow, on rear)
Front Panel Header	▶ 1x Header Reset Button, HDD LED & External Buzzer ▶ 1x Header for Power Button, Power LED & SM Bus
Cooling	
FAN	▶ 1x Wafer for Smart Fan
Software	
OS Support	▶ Windows 11 ▶ Windows 10 ▶ Linux
Mechanical	
Dimension (L x W)	▶ ECX (146 mm x 105 mm / 5.75" x 4.13")

3.3. Environmental Conditions

The 3.5"-SBC-RPL is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

Operating Temperature	▶ 0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard) ▶ -40 °C ~ 85 °C / -40 °F ~ 185 °F (Extreme)
Storage Temperature	▶ -20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard) ▶ -55 °C ~ 85 °C / -67 °F ~ 185 °F (Extreme)

Humidity	0 % ~ 95 %

3.4. Standards and Certifications

The 3.5"-SBC-RPL meets the following standards and certification tests.

Table 3: Standards and Certifications

CE Class B UKCA	TBD
FCC Class B ICES Class B	TBD
UR (UL Recognized)	TBD

3.5. Processor Support

The 3.5"-SBC-RPL is designed to support 13th Gen Intel® Core™ U-Series and Intel® U300E Processors. The BGA CPU is remounted from factory. Kontron has defined the CPU SKUs as listed in the following table for either standard or project-based board versions, so far all based on Embedded CPUs. Other CPU SKUs are expected at a later date.

Table 4: Processor Support

Name	Core #		Speed (GHz)	Turbo (GHz)	Emb.	Cache	Socket	TDP (W)			Tj (°C)
	Perf.	Eff.						Base	Up	Dn	
Intel® Core™ i7-1365UE	2	8	1.7	4.9	Yes	12M	BGA1744	15	28	12	100
Intel® Core™ i5-1345UE	2	8	1.4	4.6	Yes	12M	BGA1744	15	28	12	100
Intel® Core™ i3-1315UE	2	4	1.2	4.5	Yes	10M	BGA1744	15	28	12	100
Intel® Core™ i7-1365URE	2	8	1.7	4.9	Yes	12M	BGA1744	15	28	12	100
Intel® Core™ i5-1345URE	2	8	1.4	4.6	Yes	12M	BGA1744	15	28	12	100
Intel® Core™ i3-1315URE	2	4	1.2	4.5	Yes	10M	BGA1744	15	28	12	100
Intel® U300E	1	4	1.1	4.3	Yes	8M	BGA1744	15	28	12	100

Sufficient cooling must be applied to the CPU in order to remove the effect as listed as TDP (Thermal Design Power) in above table. The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

3.6. System Memory Support

The 3.5"-SBC-RPL has two DDR5 SO-DIMM sockets. The sockets support the following memory features:

- 2x DDR5 SO-DIMM 262-pin
- Dual-channel with 1x SO-DIMM per channel
- Up to 96 GB
- SPD timing supported
- In-band ECC supported for Core™ URE Series processors

The installed DDR5 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of SO-DIMMs and processor.

Table 5: Memory Operating Frequencies

SO-DIMM Type	Module Name	Memory Data Transfer (MT/s)	Processor System Bus Frequency (MHz)	Resulting Memory Clock Frequency (MHz)	Peak Transfer Rate (MB/s)
DDR5 5200	PC5-41600	5200	2600	325	41600

Memory modules have in general a much lower longevity than the embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

3.7. On-board Graphics Subsystem

The 3.5"-SBC-RPL supports Intel® Iris® Xᵉ Graphics technology for high quality graphics capabilities. All 3.5"-SBC-RPL versions support quadruple displays pipes.

Quadruple displays can be used simultaneously and be used to implement independent or cloned display configuration.

The 3.5"-SBC-APL itself provides one internal eDP / LVDS combo interface and two external DisplayPort connectors. It additionally supports a DDI (Digital Display Interface) signal and a DDI TCP (Type C Port) signal via the extended board-to-board connector (CN14). The DDI signal can support an internal eDP interface or an external DisplayPort conenctor; the DDI TCP signal can support an external DisplayPort or DisplayPort over USB Type C connector.

Table 6: Quadruple-displays Configurations

Display 1	Display 2	Display 3	Display 4	Max. Resolution (Px) at 60 Hz			
				Display 1	Display 2	Display 3	Display 4
eDP	DP	DP	DDI	4096 x 2304*	7680 x 4320	7680 x 4320	7680 x 4320
eDP	DP	DP	DDI TCP	4096 x 2304*	7680 x 4320	7680 x 4320	7680 x 4320
eDP	DP	DDI	DDI TCP	4096 x 2304*	7680 x 4320	7680 x 4320	7680 x 4320
LVDS	DP	DP	DDI	1920 x 1200	7680 x 4320	7680 x 4320	7680 x 4320
LVDS	DP	DP	DDI TCP	1920 x 1200	7680 x 4320	7680 x 4320	7680 x 4320
LVDS	DP	DDI	DDI TCP	1920 x 1200	7680 x 4320	7680 x 4320	7680 x 4320
DP	DP	DDI	DDI TCP	7680 x 4320	7680 x 4320	7680 x 4320	7680 x 4320

* Max. resolution at 120 Hz

3.8. Power Supply Voltage

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. The 3.5"-SBC-RPL board must be powered through the 3.0 mm pitch 1x4-pin wafer connector from a single DC power supply. Depending on the ordered 3.5"-SBC-RPL configuration, the input voltage must be either DC 12 V or a value within the range between 9 V and 36 V .

NOTICE

Hot Plugging power supply is not supported. Hot plugging might damage the board.

The requirements to the supply voltages are as follows:

Table 7: Supply Voltages

Supply	Min.	Max.	Note
9 V ~ 36 V	8.55 V	37.8 V	Should be ±5 % tolerance
12 V	11.4 V	12.6 V	Should be ±5 % tolerance

3.9. Power Consumption

The power consumption is measured under the following software and hardware test condition.

- 3.5"-SBC-RPL with Intel® Core™ i7-1365URE processor (Deca Core @ 4.9 GHz)
- Memory: 1x 16 GByte TEAMGROUP DDR5 5600 RAM
- Storage: 128 GByte Phison M.2 SATA SSD
- Operating System: Windows 10 IoT LTSC 21H2

The power consumption in different modes is as follows:

Table 8: Power Consumption

Mode	Voltage	Power Consumption	
		Peak	Mean
Boot	+36 V	179.2 W	31 W
	+12 V	90.7 W	37.7 W
Idle (S0)	+36 V	185.4 W	12.8 W
	+12 V	48.7 W	6.1 W
Full Run (S0)	+36 V	188.3 W	15 W
	+12 V	97.2 W	39.4 W
Sleep (S3)	+36 V	20.1 W	1.7 W
	+12 V	7.4 W	1.4 W
Shutdown (S4 / S5)	+36 V	15 W	1.2 W
	+12 V	5 W	1.1 W

4/ Connector Locations

4.1. Top Side

Figure 2: Top Side

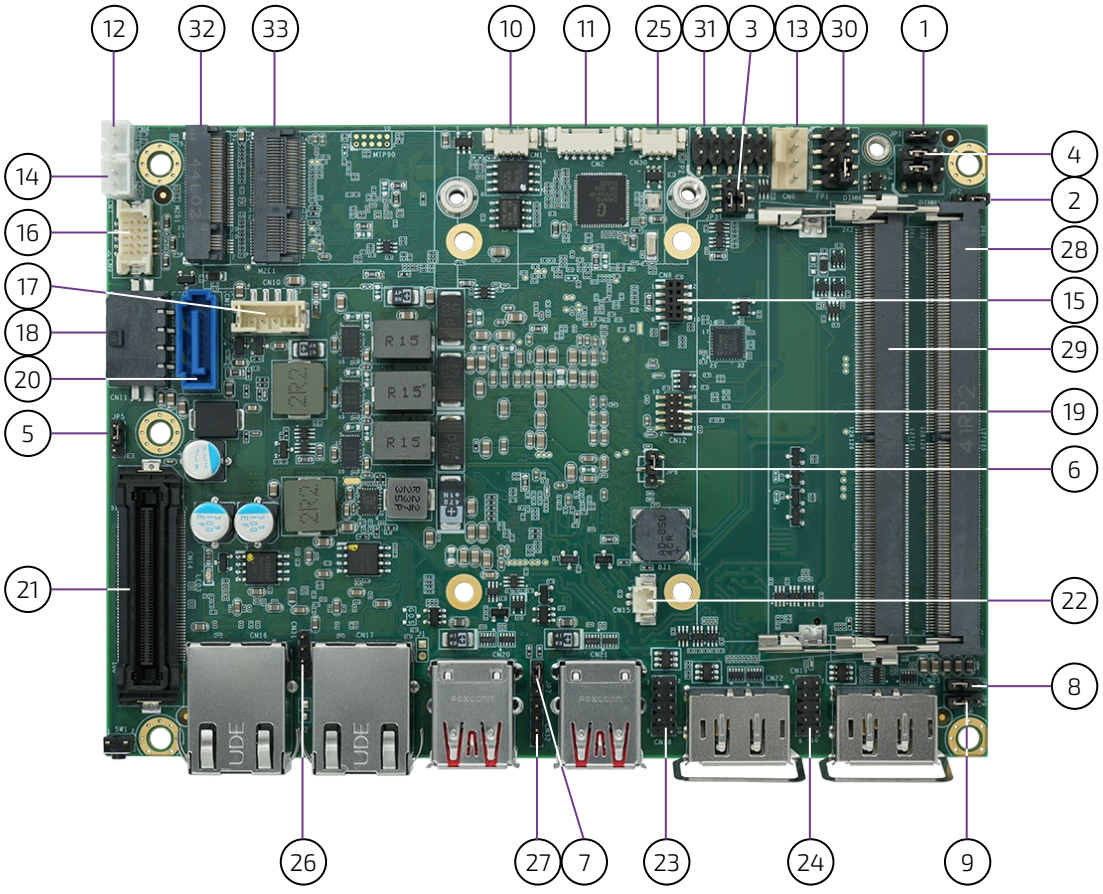


Table 9: Jumper List

Item	Designation	Description	See Chapter
1	JP1	Power Mode Selection	7.23.1
2	JP2	AT / ATX Power Mode Selection	7.23.2
3	JP3	eDP / LVDS Backlight Enable Voltage Selection	7.23.3
4	JP4	eDP / LVDS Backlight Power & Panel Power Selection	7.23.4
5	JP5	Flash Descriptor Security Override Selection	7.23.5
6	JP6	M.2 Key B Selection	7.23.6
7	JP7	USB Power Selection	7.23.7
8	JP8	MFG Mode Selection	7.23.8
9	JP9	Clear CMOS Selection	7.23.9

Table 10: Top Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
10	CN1	S/PDIF Output Wafer	7.8
11	CN2	SIM Card Wafer for M.2 Key B	7.20
12	CN4	Left Channel Audio AMP Output Wafer	7.6
13	CN6	FAN Wafer	7.2
14	CN7	Right Channel Audio AMP Output Wafer	7.6
15	CN8	P80 Holder	-
16	CN9	Audio Input / Output Header	7.7
17	CN10	SATA Power Output Wafer	7.4
18	CN11	Power Input Wafer	7.1.1
19	CN12	SPI 10-Pins Header	7.16
20	CN13	SATA Connector	7.3
21	CN14	Board-to-board Connector	7.22
22	CN15	RTC Power Input Wafer	7.1.2
23	CN18	USB 2.0 Port 5 & 6 Header	7.5
24	CN19	USB 2.0 Port 7 & 8 Header	7.5
25	CN30	LVDS Backlight Control Wafer	7.13
26	CN31	2.5 GbE LAN1 LED Indicator Header	7.21
27	CN32	2.5 GbE LAN2 LED Indicator Header	7.21
28	DIMM1	DDR5 Channel 1 SO-DIMM Slot	3.6
29	DIMM2	DDR5 Channel 2 SO-DIMM Slot	3.6
30	FP1	Front Panel Header 1	7.9
31	FP2	Front Panel Header 2	7.9
32	M2B1	M.2 Key B 2242 / 3042 / 3052 / 2280 Slot	7.17
33	M2E1	M.2 Key E 2230 Slot	7.18

4.2. Rear Side

Figure 3: Rear Side

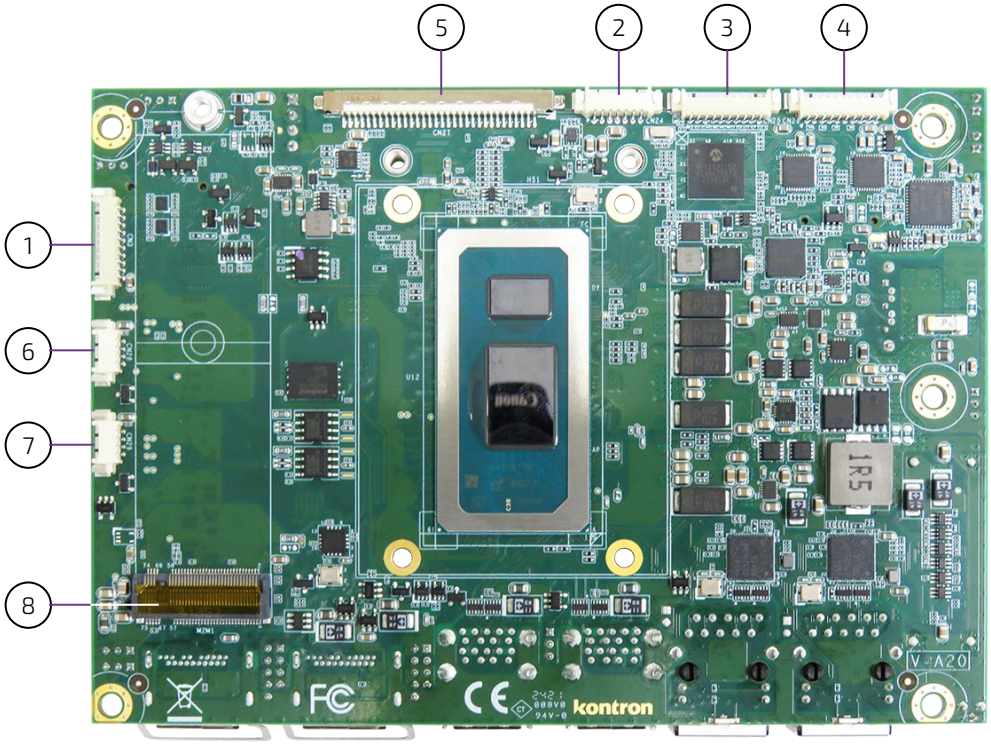


Table 11: Rear Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
1	CN3	DIO Wafer	7.14
2	CN24	eDP / LVDS Backlight Power Wafer	7.12
3	CN25	RS232/422/485 COM2 Wafer	7.10
4	CN26	RS232/422/485 COM1 Wafer	7.10
5	CN27	eDP / LVDS Combo Connector	7.11
6	CN28	CAN Bus Port 1 Wafer (Optional)	7.15
7	CN29	CAN Bus Port 2 Wafer (Optional)	7.15
8	M2M1	M.2 Key M 2280 Slot	7.19

4.3. Connector Panel Side

Figure 4: Connector Panel Side

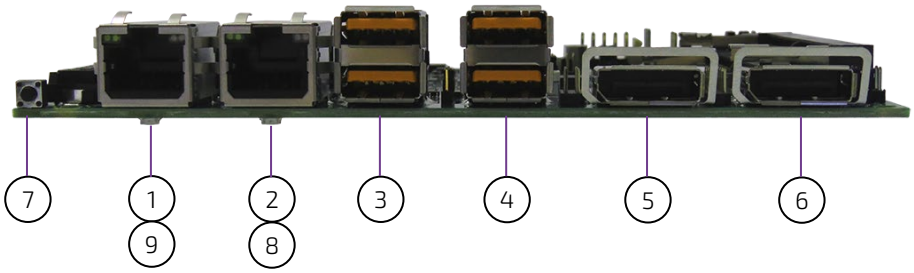


Table 12: Connector Panel Side Connector List

Item	Designation	Description	See Chapter
1	CN16	2.5 GbE LAN1 RJ45 Connector	6.1
2	CN17	2.5 GbE LAN2 RJ45 Connector	6.1
3	CN20	USB 3.2 Gen 2 Port 1, 2 Type A Connector	6.3
4	CN21	USB 3.2 Gen 2 Port 3, 4 Type A Connector	6.3
5	CN22	DP Port 1 Connector	6.2
6	CN23	DP Port 2 Connector	6.2
7	SW1	Power Button	6.4
8	LED1	Standby LED	6.5
9	LED2	Power LED	6.5

5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin The notation "XX#" states that the signal "XX" is active low
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

6/ I/O-Area Connectors

6.1. Ethernet Connectors (CN16 & CN17)

The 3.5"-SBC-RPL supports two channels of 10/100/1000/2500 Mbit Ethernet, which are based Intel® I226-LM/IT controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit/2.5 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 5: Ethernet Connector CN16, CN17

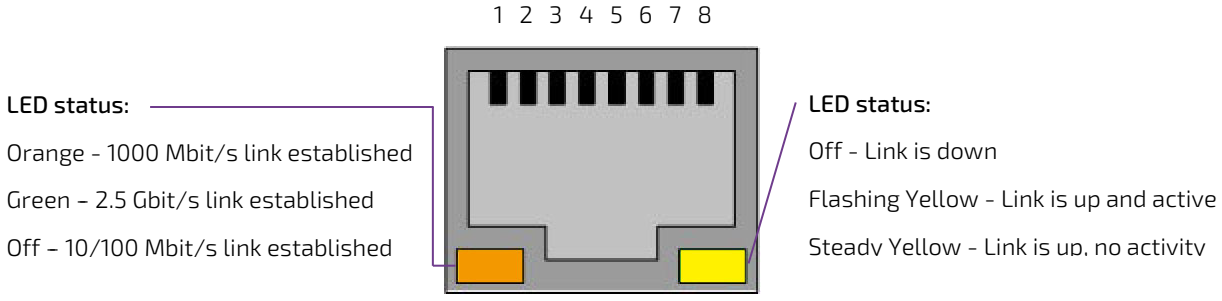


Table 13: Pin Assignment Ethernet Connectors CN16, CN17

Pin	Signal	Note
1	TX1+	
2	TX1-	
3	TX2+	
4	TX3+	
5	TX3-	
6	TX2-	
7	TX4+	
8	TX4-	

Signal Description

Signal	Description
TX1+ / TX1-	In MDI mode, this is the first pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
TX2+ / TX2-	In MDI mode, this is the second pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
TX3+ / TX3-	In MDI mode, this is the third pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
TX4+ / TX4-	In MDI mode, this is the fourth pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair.

'MDI' – media dependent Interface

6.2. DP Connector (CN22 & CN23)

The DP (DisplayPort) connectors are based on standard DP female port.

Figure 6: DP Connector CN22, CN23

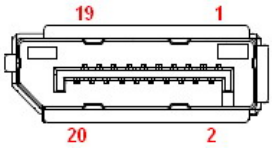


Table 14: Pin Assignment DP Connector CN22, CN23

Pin	Signal	Description	Note
1	ML_Lane0p	DisplayPort Lane 0 transmitter differential pair (+)	
2	GND	Ground	
3	ML_Lane0n	DisplayPort Lane 0 transmitter differential pair (-)	
4	ML_Lane1p	DisplayPort Lane 1 transmitter differential pair (+)	
5	GND	Ground	
6	ML_Lane1n	DisplayPort Lane 1 transmitter differential pair (-)	
7	ML_Lane2p	DisplayPort Lane 2 transmitter differential pair (+)	
8	GND	Ground	
9	ML_Lane2n	DisplayPort Lane 2 transmitter differential pair (-)	
10	ML_Lane3p	DisplayPort Lane 3 transmitter differential pair (+)	
11	GND	Ground	
12	ML_Lane3n	DisplayPort Lane 3 transmitter differential pair (-)	
13	Config1	Connected to ground, either directly or through a pulldown device	
14	Config2	Connected to ground, either directly or through a pulldown device	
15	AUX_CHp	DisplayPort Auxiliary channel differential pair (+)	
16	GND	Ground	
17	AUX_CHn	DisplayPort Auxiliary channel differential pair (-)	
18	Hot_Plug	DisplayPort hot plug detect	
19	GND	Ground	
20	DP_PWR	Power for connector	

6.3. USB Connectors (I/O Area)

The external I/O connector panel supports two dual USB 3.2 Gen 2 connectors (CN20 & CN21).

USB 3.2 Gen 2 ports are backward compatible with USB 3.2 Gen 1 and USB 2.0.

Figure 7: USB 3.2 Gen 2 Connectors CN20 – Top & Bottom, CN21 – Top & Bottom

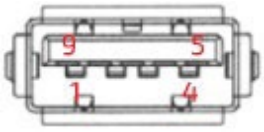


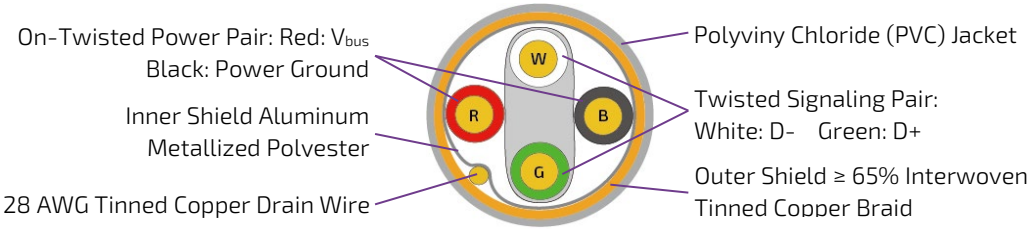
Table 15: Pin Assignment USB 3.2 Gen 2 Connectors CN20 – Top & Bottom, CN21 – Top & Bottom

Pin	Signal	Description	Note
1	+USB_VCC*	+5 V power supply for USB device	
2	USB_D-	USB 2.0 differential pair (-)	
3	USB_D+	USB 2.0 differential pair (+)	
4	GND	Ground	
5	USB_RX-	USB 3.2 receiver differential pair (-)	
6	USB_RX+	USB 3.2 receiver differential pair (+)	
7	GND	Ground	
8	USB_TX-	USB 3.2 transmitter differential pair (-)	
9	USB_TX+	USB 3.2 transmitter differential pair (+)	

*** The power source of +USB_VCC can be selected through JP7.**

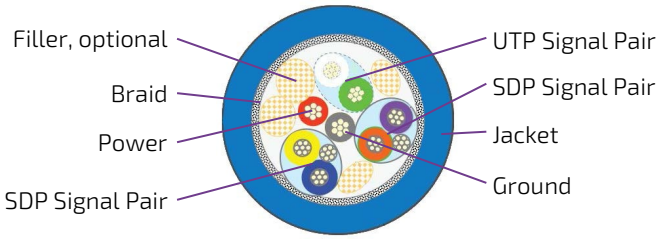
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 8: USB 2.0 High Speed Cable



For USB 3.2 Gen 2 cabling it is required to use only HiSpeed USB cable, specified in USB 3.2 standard:

Figure 9: USB 3.2 High Speed Cable



6.4. Power Button (SW1)

The external I/O connector panel supports a power button (SW1) for turning on and off the board.

6.5. LED Indicators (LED1 & LED2)

The external I/O connector panel supports one power LED indicator (LED2) and one standby LED indicator (LED1) for power and standby status indication.

Table 16: LED Indicators LED1, LED2

LED Status		Description
Power LED (LED2)	Standby LED (LED1)	
Green LED On	Yellow LED On	S0 (Full On)
Green LED Blink	Yellow LED On	S3 (Suspend-To-RAM)
LED Off	Yellow LED On	S4 (Suspend-To-Disk) or S5 (Soft Off)
LED Off	LED Off	EUP Mode or G3 (Mechanical Off)

7/ Internal Connectors

7.1. Power Connector

Depending on the ordered 3.5"-SBC-RPL configuration, the power connector must be used to supply the board with a single DC power of either 12 V or a value within the range between 9 V and 36 V (±5 %).

NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

7.1.1. Power Input Wafer (CN11)

The 1x4-pin 3.0 mm pitch power input wafer CN11 provides a single DC power of either 12 V or a value within the range between 9 V and 36 V to the board depending on the ordered configuration.

Figure 10: Power Input Wafer CN11

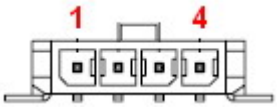


Table 17: Pin Assignment CN11

Pin	Signal	Description	Note
1	+Vin	Power input	
2	GND	Ground	
3	GND	Ground	
4	+Vin	Power input	
Connector Type			
B2W, 1x4-pin, 3.0 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	733-75-M104B6		
Terminal Model No.	733-70-FT0006		

7.1.2. RTC Power Input Wafer (CN15)

The 1x2-pin 1.25 mm pitch RTC power input wafer CN15 is intended to be connected to the battery. The battery provides power to the system clock to retain the time when power is turn off.

Figure 11: RTC Power Input Wafer CN15

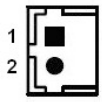


Table 18: Pin Assignment CN15

Pin	Signal	Description	Note
1	+VRTC	Real-time clock backup battery input	
2	GND	Ground	
Connector Type			
B2W, 1x2-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-02W001		
Terminal Model No.	712-70-T00001		

7.2. Fan Wafer (CN6)

The 1x4-pin 2.54 mm pitch fan wafer CN6 is used for the connection of the fan for the processor or system.

Figure 12: Fan Wafer CN6

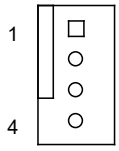


Table 19: Pin Assignment CN6

Pin	Signal	Description	Note
1	GND	Power supply ground signal	
2	+12V	+12 V power supply for fan	1 A max.
3	SENSE	Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute).	
4	PWM	PWM output signal for FAN speed control	
Connector Type			
B2W, 1x4-pin, 2.54 mm pitch			

7.3. SATA (Serial ATA) Connector (CN13)

The SATA connector CN13 supplies the data connection for the SATA hard disk and is SATA 3.0 compatible.

Figure 13: SATA Connector CN13

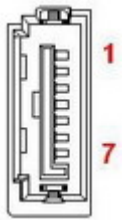


Table 20: Pin Assignment CN13

Pin	Signal	Description	Note
1	GND	Ground	
2	TX+	Host transmitter differential signal pair (+)	
3	TX-	Host transmitter differential signal pair (-)	
4	GND	Ground	
5	RX-	Host receiver differential signal pair (-)	
6	RX+	Host receiver differential signal pair (+)	
7	GND	Ground	
Connector Type			
B2W, 1x7-pin, 1.27 mm pitch			
Mating Connector			
Vendor	WINWIN		
Model No.	WATC-07DLPO2U		

7.4. SATA Power Output Wafer (CN10)

The 1x4-pin 2.0 mm pitch SATA power output wafer CN10 provides power to the SATA hard disk.

Figure 14: SATA Power Output Wafer CN10

Table 21: Pin Assignment CN10

Pin	Signal	Description	Note
1	+12V	+12 V power supply for HDD / SSD	1.5 A max.
2	GND	Ground	
3	GND	Ground	
4	+5V	+5 V power supply for HDD / SSD	1.5 A max.
Connector Type			
B2W, 1x4-pin, 2.0 mm pitch			
Mating Connector			
Vendor **Housing Model No.** **Terminal Model No.**	Pinrex 721-75-04W009 721-70-T00009		

7.5. USB Connectors (Internal) (CN18 & CN19)

The 10-pin 2.0 mm pitch USB port header CN18 supports two USB 2.0 ports, Port 5 and Port 6. The USB signals of two ports are shared with those reserved on the board-to-board connector (CN14) and may be traded off optionally based on the request.

The 10-pin 2.0 mm pitch USB port header CN19 supports two USB 2.0 ports, Port 7 and Port 8. The USB signals of Port 8 (Channel B) are shared with those to CAN Bus controller for two CAN Bus wafers (CN28 & CN29) and may be traded off optionally based on the request.

Figure 15: USB 2.0 Port 5, 6 Header CN18, Port 7, 8 Header CN19

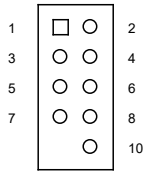


Table 22: Pin Assignment CN18, CN19

Pin	Signal	Description	Note
1	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	500 mA max.
2	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	500 mA max.
3	USB_DA-	USB 2.0 differential pair (-) for channel A	
4	USB_DB-	USB 2.0 differential pair (-) for channel B	
5	USB_DA+	USB 2.0 differential pair (+) for channel A	
6	USB_DB+	USB 2.0 differential pair (+) for channel B	
7	GND	Ground	
8	GND	Ground	
9	KEY		
10	GND	Ground	
Connector Type			
B2W, 2x5-pin, 2.0 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	720-75-205B03		
Terminal Model No.	720-70-G00013		

* The power source of +USBVCC can be selected through JP7.

7.6. Audio AMP Output Wafer (CN4 & CN7)

The Speaker audio-out interface is available through the 2-pin 2.0 mm pitch wafers CN4 for left channel and CN7 for right channel. These outputs are shared with the audio output (Line-out) signals of the audio pin header CN9.

Figure 16: Audio AMP Output Wafer CN4 (Left Channel), CN7 (Right Channel)

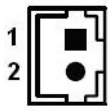


Table 23: Pin Assignment CN4, CN7

Pin	Signal	Description	Note
1	Speaker+	Speaker output (+)	
2	Speaker-	Speaker output (-)	
Connector Type			
B2W, 1x2-pin, 2.0 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	721-75-02W009		
Terminal Model No.	721-70-T00009		

7.7. Audio Input / Output Header (CN9)

The 10-pin 1.25 mm pitch audio input / output header CN9 provides audio output (Line-Out), audio input (Line-In) and microphone (Mic-In) signals. The audio output signals are shared with those of the speaker connectors CN4 & CN7.

Figure 17: Audio Input / Output Header CN9

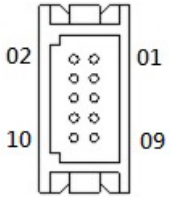


Table 24: Pin Assignment CN9

Pin	Signal	Description	Note
1	MIC-In_L	Microphone input left channel signal	
2	MIC-In_R	Microphone input right channel signal	
3	MIC-In_JD#	Microphone jack detection	
4	Line-In_JD#	Audio input jack detection	
5	Line-In_L	Audio input left channel signal	
6	Line-In_R	Audio input right channel signal	
7	Line-Out_L	Audio output left channel signal	
8	Line-Out_R	Audio output right channel signal	
9	Line-Out_JD#	Audio output jack detection	
10	GND	Ground	
Connector Type			
B2W, 2x5-pin, 1.25 mm pitch			
Mating Connector			
Vendor	HRS		
Housing Model No.	DF13-10DS-1.25C		
Terminal Model No.	WL1255-T-T-S		

7.8. S/PDIF Output Wafer (CN1)

The 3-pin 1.25 mm pitch S/PDIF output wafer CN1 is used to enable a S/PDIF audio output port to carry multi-channel compressed surround sound.

Figure 18: S/PDIF Output Wafer CN1

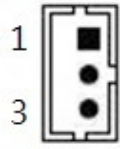


Table 25: Pin Assignment CN1

Pin	Signal	Description	Note
1	SPDIF-O	S/PDIF output	
2	+5V	5 V supply	
3	GND	Ground	
Connector Type			
B2W, 1x3-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-03W001		
Terminal Model No.	712-70-T00001		

7.9. Front Panel Header (FP1 & FP2)

The 8-pin 2.54 mm pitch front panel header FP1 supplies signals for the reset button, M.2 Key M SSD LED and system warning speaker.

The 10-pin 2.54 mm pitch front panel header FP2 supplies signals for the power button, power LED, and SM Bus.

Figure 19: Front Panel Header 1 FP1

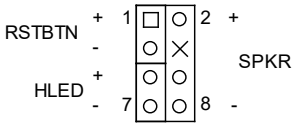


Table 26: Pin Assignment FP1

Pin	Signal	Description	Note
1	Reset Button +	System reset button (+)	
2	Speaker +	External system warning speaker (+)	
3	Reset Button -	System reset button (-)	
4	-	No connection	
5	HLED +	M.2 Key M SSD activity LED (+). The LED lights up or flashes when data is ready from or written to the SSD.	
6	Internal Speaker -	Internal system warning speaker (-)	
7	HLED -	M.2 Key M SSD activity LED (-).	
8	Speaker -	External system warning speaker (-)	
Connector Type			
B2W, 2x4-pin, 2.54 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	741-75-204B01		
Terminal Model No.	741-70-FT0001		

Internal Buzzer is enabled when Pin6-8 is shorted.

Figure 20: Front Panel Header 2 FP2

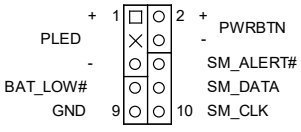


Table 27: Pin Assignment FP2

Pin	Signal	Description	Note
1	Power LED +	System Power LED (+). The LED lights up when users turn on the	

Pin	Signal	Description	Note
		system power, and blinks when the system is in sleep mode.	
2	Power Button +	System power button (+). Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF.	
3	-	No connection	
4	Power Button -	System power button (-).	
5	Power LED -	System Power LED (-).	
6	-	No connection	
7	-	No connection	
8	SMBus Data	System management bus bidirectional data line	
9	GND	Ground	
10	SMBus Clock	System management bus bidirectional clock line	
Connector Type			
B2W, 2x5-pin, 2.54 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	741-75-205B01		
Terminal Model No.	741-70-FT0001		

7.10. Serial COM1 & COM2 Ports (CN26 & CN25)

The 10-pin 1.25 mm pitch serial COM wafers CN25 and CN26 provide RS232/422/485 connections.

All wafers support RS232 without hardware flow control.

Figure 21: Serial COM CN25, CN26

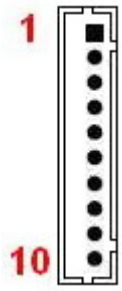


Table 28: Pin Assignment COM1 CN26, COM2 CN25

Pin	RS232 Signal	RS422 Signal	Half Duplex RS485 Signal	Full Duplex RS485 Signal	Note
1	DCD	TX-	DATA-	TX-	
2	-	-	-	-	
3	RXD	TX+	DATA+	TX+	
4	-	-	-	-	
5	TXD	RX+	-	RX+	
6	-	-	-	-	
7	DTR	RX-	-	RX-	
8	-	-	-	-	
9	GND	GND	GND	GND	
10	+5V	+5V	+5V	+5V	500 mA max.
Connector Type					
B2W, 1x10-pin, 1.25 mm pitch					
Mating Connector					
Vendor Pinrex **Housing Model No.** 712-75-10W001 **Terminal Model No.** 712-70-T00001					

Table 29: Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.

Signal	Description
TX+/-	Transmitted Data differential pair sends data to the communications link.
RX+/-	Received Data differential pair receives data from the communications link.
DATA+/-	Transmitted / Received Data differential pair sends / received data to / from the communications link.
GND	Power Supply GND signal

7.11. eDP / LVDS Combo Connector (CN27)

The 30-pole 1.0 mm pitch connector CN27 provides either eDP or 24-bit, 2-channel LVDS panel connection. The switch between eDP mode and LVDS mode can be configured in the BIOS settings.

Figure 22: eDP / LVDS Combo Connector CN27

Table 30: Pin Assignment CN27

Pin	Signal		Description		Note
	LVDS Mode	eDP Mode	LVDS Mode	eDP Mode	
1	LVDSA_TX0-	-	LVDS Ch. A Data 0 diff. pair (-)	-	
2	LVDSA_TX0+	-	LVDS Ch. A Data 0 diff. pair (+)	-	
3	LVDSA_TX1-	eDP_TX1-	LVDS Ch. A Data 1 diff. pair (-)	eDP Lane 1 diff. pair (-)	
4	LVDSA_TX1+	eDP_TX1+	LVDS Ch. A Data 1 diff. pair (+)	eDP Lane 1 diff. pair (+)	
5	LVDSA_TX2-	eDP_TX0-	LVDS Ch. A Data 2 diff. pair (-)	eDP Lane 0 diff. pair (-)	
6	LVDSA_TX2+	eDP_TX0+	LVDS Ch. A Data 2 diff. pair (+)	eDP Lane 0 diff. pair (+)	
7	GND		Ground		
8	LVDSA_BCLK-	eDP_AUX-	LVDS Ch. A clock diff. pair (-)	eDP aux. ch. diff. pair (-)	
9	LVDSA_BCLK+	eDP_AUX+	LVDS Ch. A clock diff. pair (+)	eDP aux. ch. diff. pair (+)	
10	LVDSA_TX3-	-	LVDS Ch. A Data 3 diff. pair (-)	-	
11	LVDSA_TX3+	-	LVDS Ch. A Data 3 diff. pair (+)	-	
12	LVDSB_TX0-	-	LVDS Ch. B Data 0 diff. pair (-)	-	
13	LVDSB_TX0+	-	LVDS Ch. B Data 0 diff. pair (+)	-	
14	GND		Ground		
15	LVDSB_TX1-	-	LVDS Ch. B Data 1 diff. pair (-)	-	
16	LVDSB_TX1+	-	LVDS Ch. B Data 1 diff. pair (-)	-	
17	GND		Ground		
18	LVDSB_TX2-	-	LVDS Ch. B Data 2 diff. pair (-)	-	
19	LVDSB_TX2+	-	LVDS Ch. B Data 2 diff. pair (+)	-	
20	LVDSB_BCLK-	-	LVDS Ch. B clock diff. pair (-)	-	

Pin	Signal		Description		Note
	LVDS Mode	eDP Mode	LVDS Mode	eDP Mode	
21	LVDSB_BCLK+	-	LVDS Ch. B clock diff. pair (+)	-	
22	LVDSB_TX3-	-	LVDS Ch. B Data 3 diff. pair (-)	-	
23	LVDSB_TX3+	-	LVDS Ch. B Data 3 diff. pair (+)	-	
24	GND		Ground		
25	-	eDP_HPD	-	eDP hot plug detect	
26	VDDEN	VDDEN	Output display enable	Output display enable	
27	-	-	-	-	
28	+VPNL *		+3.3 V / +5 V panel power supply		500 mA max.
29	+VPNL *		+3.3 V / +5 V panel power supply		500 mA max.
30	+VPNL *		+3.3 V / +5 V panel power supply		500 mA max.
Connector Type					
B2W, 1x30-pin, 1.0 mm pitch					
Mating Connector					
Vendor	JAE				
Model No.	FI-X30HL				

* **Panel Power can be selected through JP4.**

7.12. eDP / LVDS Backlight Power Wafer (CN24)

The 7-pin 1.25 mm pitch wafer CN24 provides power supply for flat panel and its backlight inverter.

Figure 23: eDP / LVDS Backlight Power Wafer CN24

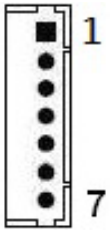


Table 31: Pin Assignment CN24

Pin	Signal	Description	Note
1	BL_EN*	Backlight Enable signal	
2	GND	Ground	
3	+VBKLT**	+5 V / +12 V backlight power supply	750 mA max.
4	+VBKLT**	+5 V / +12 V backlight power supply	750 mA max.
5	GND	Ground	
6	NC	Non connection	
7	BL_ADJ_PWM	Backlight Adjustment PWM (Pulse Width Modulation) signal	
Connector Type			
B2W, 1x7-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-07W001		
Terminal Model No.	712-70-T00001		

* **BL_EN can be selected through JP3.**

** **Backlight Power can be selected through JP4.**

7.13. eDP / LVDS Backlight Control Wafer (CN30)

The 3-pin 1.25 mm pitch wafer CN30 provides signals for backlight brightness level adjustment.

Figure 24: eDP / LVDS Backlight Control Wafer CN30

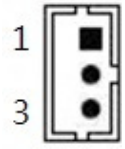


Table 32: Pin Assignment CN30

Pin	Signal	Description	Note
1	LVDS_BLUP	Increase eDP / LVDS backlight brightness level	
2	LVDS_BLDN	Decrease eDP / LVDS backlight brightness level	
3	GND	Ground	
Connector Type			
B2W, 1x3-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-03W001		
Terminal Model No.	712-70-T00001		

7.14. Digital Input / Output Header (CN3)

The 10-pin 1.25 mm pitch header CN3 supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

Figure 25: Digital Input / Output Header CN3

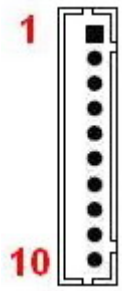


Table 33: Pin Assignment CN3

Pin	Signal	Description	Note
1	+5V	+5 V power supply	500 mA max.
2	DIO_0	Digital input / output channel 0	
3	DIO_1	Digital input / output channel 1	
4	DIO_2	Digital input / output channel 2	
5	DIO_3	Digital input / output channel 3	
6	DIO_4	Digital input / output channel 4	
7	DIO_5	Digital input / output channel 5	
8	DIO_6	Digital input / output channel 6	
9	DIO_7	Digital input / output channel 7	
10	GND	Ground	
Connector Type			
B2W, 1x10-pin, 1.25 mm pitch			
Mating Connector			
Vendor	Pinrex		
Housing Model No.	712-75-10W001		
Terminal Model No.	712-70-T00001		

7.15. CAN Bus Wafer (CN28 & CN29) (Optional)

The optional 4-pin 1.25 mm pitch wafers CN28 and CN29 support CAN Bus ports to connect sensors and controllers (Electronic Control Units - ECUs) within an automotive or industrial CAN communication network.

The CAN Bus functionality works through an optional USB to CAN Bus controller mounted on the mainboard. The USB signals to the controller are shared with those on the Channel B (Port 8) of USB Port Header CN19. If a customer requires the CAN Bus functionality, it must be so stipulated when ordering, as the CAN Bus controller and wafers must be mounted at the factory as well as appropriate signal routing by trading off an internal USB 2.0 connectivity.

Figure 26: CAN Bus Wafer CN28, CN29

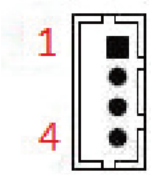


Table 34: Pin Assignment CN28, CN29

Pin	Signal	Description	Note
1	GND	Ground	
2	CAN_H	CAN high bus line	
3	CAN_L	CAN low bus line	
4	+5V_S0	+5 V power supply	500 mA max.
Connector Type			
B2W, 1x4-pin, 1.25 mm pitch			
Mating Connector			
Vendor Pinrex **Housing Model No.** 712-75-4W001 **Terminal Model No.** 712-70-T00001			

The function of CAN Bus works only under Linux OS.

7.16. SPI 10-Pins Header (CN12)

The 10-pin 1.27 mm pitch header CN12 allows connection with a MCU (MicroController Unit) module for a particular application.

Figure 27: SPI 10-Pins Header CN12

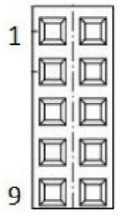


Table 35: Pin Assignment CN12

Pin	Signal	Description	Note
1	VDD	Primary supply input	
2	GND	Ground	
3	CS1#	SPI slave chip select bit 1	
4	CS0#	SPI slave chip select bit 0	
5	HOLD#	SPI HOLD	
6	SO	SPI slave serial data output	
7	SCK	SPI clock input	
8	WP#	Write-protect pin	
9	SI	SPI slave serial data input	
10	EN	Enable pin	
Connector Type			
B2B, 2x5-pin, 1.27 mm pitch			

7.17. M.2 Key B 2242 / 3042 / 3052 / 2280 Slot (M2B1)

The 3.5"-SBC-RPL supports a M.2 module in format 2242 / 3042 / 3052 / 2280 with Key B. The M.2 specification supports PCIe x1, SATA 3.0 and USB 2.0 signals as well as UIM signals connected to SIM card wafer CN2. The slot can be used to integrate WWAN communication or other possible function to the mainboard.

Figure 28: M.2 Key B 2242 / 3042 / 3052 / 2280 Slot M2B1

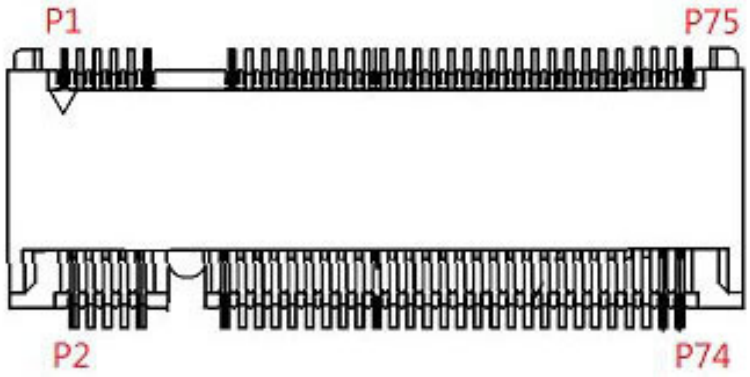


Table 36: Pin Assignment M2B1

Pin	Signal	Description	Note
1	-		
2	+3.3V	3.3 V power supply	
3	GND	Ground	
4	+3.3V	3.3 V power supply	
5	GND	Ground	
6	PWROFF#	M.2 module power enable	
7	USB_D+	USB 2.0 data differential pair (+)	
8	DISABLE#	Wireless disable	
9	USB_D-	USB 2.0 data differential pair (-)	
10	-		
11	GND	Ground	
12	KEY		
13	KEY		
14	KEY		
15	KEY		
16	KEY		
17	KEY		
18	KEY		
19	KEY		
20	-		
21	-		
22	-		
23	-		

Pin	Signal	Description	Note
24	-		
25	-		
26	-		
27	GND	Ground	
28	-		
29	-		
30	UIM_RESET*	SIM card reset	
31	-		
32	UIM_CLK*	SIM card clock	
33	GND	Ground	
34	UIM_DATA*	SIM card data	
35	-		
36	UIM_PWR*	SIM card power	
37	-		
38	-		
39	GND	Ground	
40	-		
41	PERn0 / SATA_B+**	PCIe Lane 0 receiver pair (-) / SATA transmitter pair (+)	
42	-		
43	PERp0 / SATA_B-**	PCIe Lane 0 receiver pair (+) / SATA transmitter pair (-)	
44	-		
45	GND	Ground	
46	-		
47	PETn0 / SATA_A-**	PCIe Lane 0 transmitter pair (-) / SATA receiver pair (-)	
48	-		
49	PETp0 / SATA_A+**	PCIe Lane 0 transmitter pair (+) / SATA receiver pair (+)	
50	PERST#	PCIe reset	
51	GND	Ground	
52	CLKREQ#	Reference clock request signal	
53	REFCLKn	PCIe reference clock pair (-)	
54	WAKE#	PCIe wake	
55	REFCLKp	PCIe reference clock pair (+)	
56	-		
57	GND	Ground	
58	-		
59	-		
60	-		
61	-		
62	-		
63	-		
64	-		
65	-		

Pin	Signal	Description	Note
66	SIM_DETECT	SIM card detect	
67	-		
68	SUSCLK	32.768 kHz clock supply input	
69	-		
70	+3.3V	3.3 V power supply	
71	GND	Ground	
72	+3.3V	3.3 V power supply	
73	GND	Ground	
74	+3.3V	3.3 V power supply	
75	-		

* These pins are connected to CN2 SIM card wafer directly.

** The switch between PCIe x1 and SATA mode can be configured through JP6.

7.18. M.2 Key E 2230 Slot (M2E1)

The 3.5"-SBC-RPL supports a M.2 module in format 2230 with Key E. The M.2 specification supports PCIe x1, USB 2.0, UART, PCM and / or CNVi signals. The slot can be used to integrate WLAN (Wi-Fi or CNVi Wi-Fi) and / or Bluetooth communication or other possible function to the mainboard.

Figure 29: M.2 Key E 2230 Slot M2E1

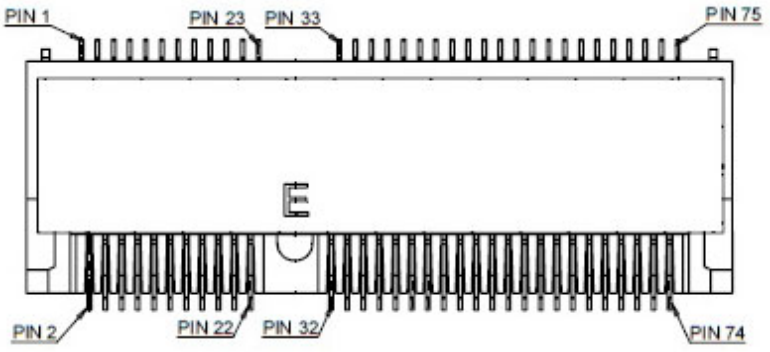


Table 37: Pin Assignment M2E1

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
1	GND	Ground	GND	Ground	
2	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
3	USB_D+	USB 2.0 data diff. pair (+)	-		
4	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
5	USB_D-	USB 2.0 data diff. pair (-)	-		
6	-		-		
7	GND	Ground	GND	Ground	
8	PCM_CLK	PCM synchronous data clock	-		
9	-		WGR_D1N	CNVio bus Rx Lane 1 (-)	
10	PCM_SYNC	PCM synchronous data sync	LCP_RSTN	RF companion (CRF) reset	
11	-		WGR_D1P	CNVio bus Rx Lane 1 (+)	
12	PCM_IN	PCM synchronous data input	-		
13	GND	Ground	GND	Ground	
14	PCM_OUT	PCM synchronous data output	CLKREQ0	Clock request	
15	-		WGR_D0N	CNVio bus Rx Lane 0 (-)	
16	-		-		
17	-		WGR_D0P	CNVio bus Rx Lane 0 (+)	
18	GND	Ground	GND	Ground	
19	GND	Ground	GND	Ground	
20	UART_WAKE#	UART wake-up	-		
21	-		WGR_CLKN	CNVio bus Rx clock (-)	
22	UART_RX	UART data input	BRI_RSP	BRI bus Rx	
23	-		WGR_CLKP	CNVio bus Rx clock (+)	

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
24	Key		Key		
25	Key		Key		
26	Key		Key		
27	Key		Key		
28	Key		Key		
29	Key		Key		
30	Key		Key		
31	Key		Key		
32	UART_TX	UART data output	RGI_DT	RGI bus Tx	
33	GND	Ground	GND	Ground	
34	UART_CTS	UART clear to send	RGI_RSP	RGI bus Rx	
35	PET0+	PCIe Lane 0 Tx pair (+)	-		
36	UART_RTS	UART request to send	BRI_DT	BRI bus Tx	
37	PET0-	PCIe Lane 0 Tx pair (-)	-		
38	Clink_RST	Wi-Fi CLINK host bus reset	-		
39	GND	Ground	GND	Ground	
40	Clink_DATA	Wi-Fi CLINK host bus data	-		
41	PER0+	PCIe Lane 0 Rx pair (+)	-		
42	Clink_CLK	Wi-Fi CLINK host bus clock	-		
43	PER0-	PCIe Lane 0 Rx pair (-)	-		
44	-		-		
45	GND	Ground	GND	Ground	
46	-		-		
47	REFCLK0+	PCIe reference clock pair (+)	-		
48	-		-		
49	REFCLK0-	PCIe reference clock pair (-)	-		
50	SUSCLK	32.768 kHz clock supply input	SUSCLK	32.768 kHz clock supply input	
51	GND	Ground	GND	Ground	
52	PERST0#	PCIe reset	-		
53	CLKREQ0#	Reference clock request signal	-		
54	W_DISABLE2#	Wireless disable 2	W_DISABLE2#	Wireless disable 2	
55	PEWAKE0#	PCIe wake	-		
56	W_DISABLE1#	Wireless disable 1	W_DISABLE1#	Wireless disable 1	
57	GND	Ground	GND	Ground	
58	-		-		
59	-		WT_D1N	CNVio bus Tx Lane 1 (-)	
60	-		-		
61	-		WT_D1P	CNVio bus Tx Lane 1 (+)	
62	-		-		
63	GND	Ground	GND	Ground	
64	-		-		

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
65	-		WT_D0N	CNVio bus Tx Lane 0 (-)	
66	PERST0#	PCIe reset	-		
67	-		WT_D0P	CNVio bus Tx Lane 0 (+)	
68	-		-		
69	GND	Ground	GND	Ground	
70	-		-		
71	-		WT_CLKN	CNVio bus Tx clock (-)	
72	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
73	-		WT_CLKP	CNVio bus Tx clock (+)	
74	+3.3V_SB	3.3 V standby power supply	+3.3V_SB	3.3 V standby power supply	
75	GND	Ground	GND	Ground	

*** The board will auto-detect the module type and re-configure itself to an appropriate mode.**

7.19. M.2 Key M 2280 Slot (M2M1)

The 3.5"-SBC-RPL ports a M.2 module in format 2280 with Key M. The M.2 specification supports PCIe x4 signal. The slot can be used to integrate a M.2 PCIe x4 SSD (NVMe) to the mainboard.

NVMe controllers are using up to 10 W (type dependent). A thermal design to compensate the heat dissipation needs to be considered.

Figure 30: M.2 Key M 2280 Slot M2M1

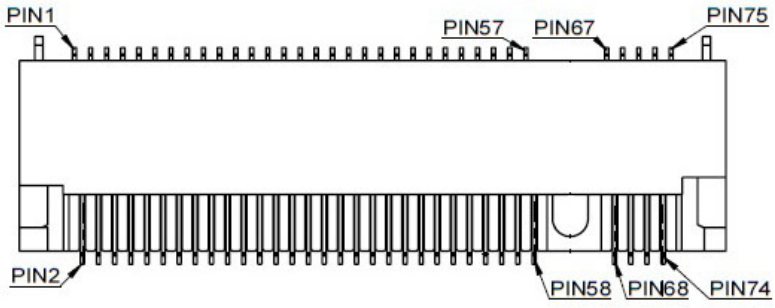


Table 38: Pin Assignment M2M1

Pin	Signal	Description	Note
1	GND	Ground	
2	+3.3V	3.3 V power supply	
3	GND	Ground	
4	+3.3V	3.3 V power supply	
5	PERn3	PCIe Lane 3 receiver pair (-)	
6	-		
7	PERp3	PCIe Lane 3 receiver pair (+)	
8	-		
9	GND	Ground	
10	DAS / DSS# / LED1#	Device active signal / disable staggered spin-up / LED	
11	PETn3	PCIe Lane 3 transmitter pair (-)	
12	+3.3V	3.3 V power supply	
13	PETp3	PCIe Lane 3 transmitter pair (+)	
14	+3.3V	3.3 V power supply	
15	GND	Ground	
16	+3.3V	3.3 V power supply	
17	PERn2	PCIe Lane 2 receiver pair (-)	
18	+3.3V	3.3 V power supply	
19	PERp2	PCIe Lane 2 receiver pair (+)	
20	-		
21	GND	Ground	
22	-		

Pin	Signal	Description	Note
23	PETn2	PCIe Lane 2 transmitter pair (-)	
24	-		
25	PETp2	PCIe Lane 2 transmitter pair (+)	
26	-		
27	GND	Ground	
28	-		
29	PERn1	PCIe Lane 1 Receiver pair (-)	
30	-		
31	PERp1	PCIe Lane 1 Receiver pair (+)	
32	-		
33	GND	Ground	
34	-		
35	PETn1	PCIe Lane 1 Transmitter pair (-)	
36	-		
37	PETp1	PCIe Lane 1 Transmitter pair (+)	
38	-		
39	GND	Ground	
40	-		
41	PERn0	PCIe Lane 0 receiver pair (-)	
42	-		
43	PERp0	PCIe Lane 0 receiver pair (+)	
44	-		
45	GND	Ground	
46	-		
47	PETn0	PCIe Lane 0 transmitter pair (-)	
48	-		
49	PETp0	PCIe Lane 0 transmitter pair (+)	
50	PERST#	PCIe reset	
51	GND	Ground	
52	CLKREQ#	Reference clock request signal	
53	REFCLKn	PCIe reference clock pair (-)	
54	PEWAKE#	PCIe wake	
55	REFCLKp	PCIe reference clock pair (+)	
56	-		
57	GND	Ground	
58	-		
59	Key		
60	Key		
61	Key		
62	Key		
63	Key		
64	Key		

Pin	Signal	Description	Note
65	Key		
66	Key		
67	-		
68	SUSCLK	32.768 kHz clock supply input	
69	PEDET	PCIe detect	
70	+3.3V	3.3 V power supply	
71	GND	Ground	
72	+3.3V	3.3 V power supply	
73	GND	Ground	
74	+3.3V	3.3 V power supply	
75	GND	Ground	

7.20. SIM Card Wafer for M.2 Key B (CN2)

The SIM card wafer CN2 is intended to enable a SIM card holder to accommodate a SIM card and connected to UIM signals on the M.2 Key B slot M2B1.

Figure 31: SIM Card Wafer CN2

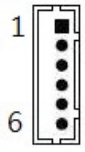


Table 39: Pin Assignment CN2

Pin	Signal	Description	Note
1	+UIM_PWR_M2B	Power +5 V or +3.3 V	
2	UIM_DATA_M2B	Input or output for serial data	
3	UIM_CLK_M2B	Clock signal	
4	UIM_RST_M2B	Reset signal	
5	UIM_CD_M2B	Card detect	
6	GND	Ground	

7.21. 2.5 GbE LAN LED Indicator Header (CN31 & CN32)

The header CN31 is intended to connect 2.5 GbE LAN1 LED indicator cable.

The header CN32 is intended to connect 2.5 GbE LAN2 LED indicator cable.

Figure 32: 2.5 GbE LAN LED Header CN31, CN32

Table 40: Pin Assignment CN31, CN32

Pin	Signal	Description	Note
1	+3.3V	+3.3 V power supply	Off – Link is down Flashing Yellow – Link is up and active Steady Yellow – Link is up, no activity
2	LAN_LINK_ACT#	LAN activity	
3	LAN_2500#	LAN 2.5 Gbit/s link	Orange – 1000 Mbit/s link established Green – 2.5 Gbit/s link established Off – 10/100 Mbit/s link established
4	LAN_1000#	LAN 1000 Mbit/s link	
Connector Type			
B2W, 1x4-pin, 2.0 mm pitch			

7.22. Board-to-board Connector (CN14)

The board-to-board connector CN14 provides connection to a daughter board for additional I/O port and / or feature expansion. The specification of the board-to-board connector supports DDI, TCP, PCIe x2, PCIe x1, SM bus, I²C, UART and GSPI signals.

The connector can support two additional USB 2.0 signals optionally by trading off USB 2.0 signals on USB 2.0 Port 5 & 6 Header (CN18) respectively. It must be so stipulated when ordering, as appropriate signal routing must be applied at the factory.

Figure 33: Board-to-board Connector CN14

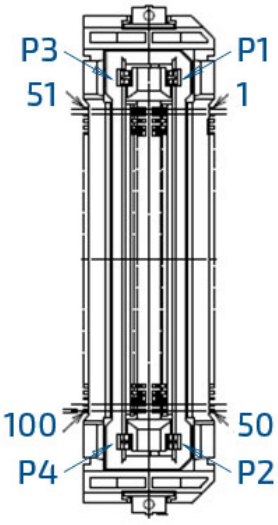


Table 41: Pin Assignment CN14

Pin	Signal	Description	Note
1	+3.3VSB_OUT	3.3 V standby power output	400 mA max.
2	+3.3VSB_OUT	3.3 V standby power output	400 mA max.
3	+3.3VSB_OUT	3.3 V standby power output	400 mA max.
4	+3.3VSB_OUT	3.3 V standby power output	400 mA max.
5	+3.3VSB_OUT	3.3 V standby power output	400 mA max.
6	GND	Ground	
7	DDI0_TXP0	DDI 0 Lane 0 transmitter pair (+)	
8	DDI0_TXN0	DDI 0 Lane 0 transmitter pair (-)	
9	GND	Ground	
10	DDI0_TXP1	DDI 0 Lane 1 transmitter pair (+)	
11	DDI0_TXN1	DDI 0 Lane 1 transmitter pair (-)	
12	GND	Ground	
13	DDI0_TXP2	DDI 0 Lane 2 transmitter pair (+)	
14	DDI0_TXN2	DDI 0 Lane 2 transmitter pair (-)	
15	GND	Ground	
16	DDI0_TXP3	DDI 0 Lane 3 transmitter pair (+)	
17	DDI0_TXN3	DDI 0 Lane 3 transmitter pair (-)	

Pin	Signal	Description	Note
18	GND	Ground	
19	DDI0_AUX+ / CLK	DDI 0 Auxiliary channel pair (+) / Clock	
20	DDI0_AUX- / DAT	DDI 0 Auxiliary channel pair (-) / Data	
21	GND	Ground	
22	PCIE0_CLK_REF+	PCIe Lane 0 clock reference pair (+)	
23	PCIE0_CLK_REF-	PCIe Lane 0 clock reference pair (-)	
24	GND	Ground	
25	PCIE0_TX+	PCIe Lane 0 transmitter pair (+)	
26	PCIE0_TX-	PCIe Lane 0 transmitter pair (-)	
27	GND	Ground	
28	PCIE0_RX+	PCIe Lane 0 receiver pair (+)	
29	PCIE0_RX-	PCIe Lane 0 receiver pair (-)	
30	GND	Ground	
31	PCIE2_TX+	PCIe Lane 2 receiver pair (+)	
32	PCIE2_TX-	PCIe Lane 2 receiver pair (-)	
33	GND	Ground	
34	PCIE2_RX+	PCIe Lane 2 receiver pair (+)	
35	PCIE2_RX-	PCIe Lane 2 receiver pair (-)	
36	GND	Ground	
37	USB0- (Reserved)	USB 2.0 differential pair (-) for channel 0	
38	USB0+ (Reserved)	USB 2.0 differential pair (+) for channel 0	
39	GND	Ground	
40	UART_TXD	UART transmitted data	
41	UART_RXD	UART received data	
42	UART_CTS#	UART clear to send	
43	UART_RTS#	UART request to send	
44	GND	Ground	
45	eDP_PWM	eDP backlight PWM (Pulse Width Modulation) signal	
46	eDP_VDDEN	eDP panel power enable signal	
47	eDP_BKLTEN	eDP backlight enable signal	
48	DP0_HPD	DP 0 hot plug detect	
49	DP0_EN#	DP 0 enable	
50	USB_OC#	Over current detect for USB	
51	GSPI_CLK	General SPI clock	
52	GSPI_MOSI	General SPI master output / slave input	
53	GSPI_MISO	General SPI master input / slave output	
54	GSPI_CS0#	General SPI chip select bit 0	
55	-		
56	GND	Ground	
57	DDI1_TXP0	DDI 1 Lane 0 transmitter pair (+)	
58	DDI1_TXN0	DDI 1 Lane 0 transmitter pair (-)	
59	GND	Ground	

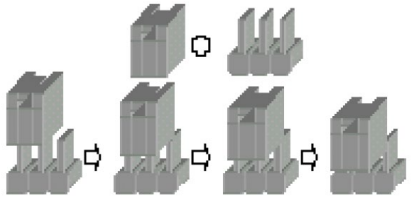
Pin	Signal	Description	Note
60	DDI1_TXP1	DDI 1 Lane 1 transmitter pair (+)	
61	DDI1_TXN1	DDI 1 Lane 1 transmitter pair (-)	
62	GND	Ground	
63	DDI1_TXP2	DDI 1 Lane 2 transmitter pair (+)	
64	DDI1_TXN2	DDI 1 Lane 2 transmitter pair (-)	
65	GND	Ground	
66	DDI1_TXP3	DDI 1 Lane 3 transmitter pair (+)	
67	DDI1_TXN3	DDI 1 Lane 3 transmitter pair (-)	
68	GND	Ground	
69	DDI1_AUX+ / CLK	DDI 1 Auxiliary channel pair (+) / Clock	
70	DDI1_AUX- / DAT	DDI 1 Auxiliary channel pair (-) / Data	
71	GND	Ground	
72	PCIE1_CLK_REF+	PCIe Lane 1 clock reference pair (+)	
73	PCIE1_CLK_REF-	PCIe Lane 1 clock reference pair (-)	
74	GND	Ground	
75	PCIE1_TX+	PCIe Lane 1 transmitter pair (+)	
76	PCIE1_TX-	PCIe Lane 1 transmitter pair (-)	
77	GND	Ground	
78	PCIE1_RX+	PCIe Lane 1 receiver pair (+)	
79	PCIE1_RX-	PCIe Lane 1 receiver pair (-)	
80	GND	Ground	
81	-		
82	-		
83	GND	Ground	
84	-		
85	-		
86	GND	Ground	
87	USB1- (Reserved)	USB 2.0 differential pair (-) for channel 1	
88	USB1+ (Reserved)	USB 2.0 differential pair (+) for channel 1	
89	GND	Ground	
90	I2C_CLK	I2C clock	
91	I2C_DATA	I2C data	
92	SMB_CLK	SM bus clock	
93	SMB_DATA	SM bus data	
94	GND	Ground	
95	SMB_ALERT#	SM bus alert	
96	PCIE_WAKE#	PCIe wake	
97	PCIE_PLTRST#	PCIe platform reset	
98	DP1_HPD	DP 1 hot plug detect	
99	DP1_EN#	DP 1 enable	
100	PS_ON#	Power supply enable / disable	
P1	+5VSB_OUT	5 V standby power output	2 A max.

Pin	Signal	Description	Note
P2	+12V_IN / +12V_OUT	12 V power input / 12 V power output	3.33 A / 0.66 A max.
P3	+12V_IN / +12V_OUT	12 V power input / 12 V power output	3.33 A / 0.66 A max.
P4	+12V_IN / +12V_OUT	12 V power input / 12 V power output	3.33 A / 0.66 A max.
Connector Type			
B2B, 2x50-pin, 0.5 mm pitch			
Mating Connector			
Vendor	HRS		
Model No.	FX23-100P-0.5SV20		

7.23. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 34: Jumper Connector



For a three-pin jumper (see Figure 34), the jumper setting is designated “1-2” when the jumper connects pins 1 and 2. The jumper setting is designated “2-3” when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

7.23.1. Power Mode Selection (JP1)

The 2.0 mm pitch "Power Mode Selection" jumper JP1 can be used to enable or disable +12 V power controller. When enabled, the board is powered from the DC power input wafer CN11; when disabled, the board is powered from the daughter board via the 12 V power pins in board-to-board connector CN14.

Figure 35: Power Mode Selection JP1

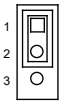


Table 42: Pin Assignment JP1

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	+12 V Controller Enable (Default)
-	X	+12 V Controller Disable

“X" = Jumper set (short) and “-” = jumper not set (open)

7.23.2. AT / ATX Power Mode Selection (JP2)

The 2.0 mm pitch jumper JP2 can be used to select AT power mode or ATX power mode.

Figure 36: AT / ATX Power Mode Selection JP2

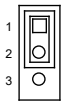


Table 43: Pin Assignment JP2

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	ATX Power Mode (Default)
-	X	AT Power Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

7.23.3. eDP / LVDS Backlight Enable Voltage Selection (JP3)

The 2.0 mm patch "eDP / LVDS Backlight Enable Voltage Selection" jumper JP3 can be used to select the voltage level and the polarity of backlight enable signal.

Figure 37: eDP / LVDS Backlight Enable Voltage Selection JP3

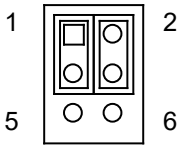


Table 44: Pin Assignment JP3

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Enable Voltage = +3.3 V
-	X	Backlight Enable Voltage = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	High Active
-	X	Low Active

"X" = Jumper set (short) and "-" = jumper not set (open)

7.23.4. eDP / LVDS Backlight & Panel Power Selection (JP4)

The 2.54 mm pitch "eDP / LVDS Backlight & Panel Power Selection" jumper JP4 can be used to select eDP / LVDS backlight and panel power voltage.

Figure 38: eDP / LVDS Backlight & Panel Power Selection JP4

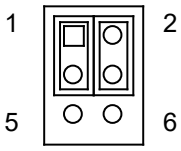


Table 45: Pin Assignment JP4

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Power = +12 V
-	X	Backlight Power = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Panel Power = +3.3 V
-	X	Panel Power = +5 V

“X" = Jumper set (short) and “-" = jumper not set (open)

7.23.5. Flash Descriptor Security Override Selection (JP5)

The 2.0 mm pitch "Flash Descriptor Security Override Selection" jumper JP5 can be used to specify whether to override the flash descriptor.

Figure 39: Flash Descriptor Security Override Selection JP5

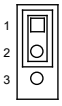


Table 46: Pin Assignment JP5

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Controlled by Embedded Controller (Default)
-	X	Flash Security Override

“X" = Jumper set (short) and “-" = jumper not set (open)

7.23.6. M.2 Key B Selection (JP6)

The 2.0 mm pitch "M.2 Key B Selection" jumper JP6 can be used to select which interface of M.2 SSD the M.2 Key B slot supports.

Figure 40: M.2 Key B Selection JP6

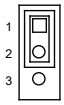


Table 47: Pin Assignment JP6

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	PCIe x1 (Default)
-	X	SATA

"X" = Jumper set (short) and "-" = jumper not set (open)

7.23.7. USB Power Selection (JP7)

The 2.0 mm pitch "USB Power Selection" jumper JP7 can be used to determine whether the USB ports are powered in the S4 / S5 state.

Figure 41: USB Power Selection JP7

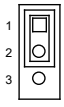


Table 48: Pin Assignment JP7

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	+5 VUSB (S0) (Default)
-	X	+5 VUSB (S5)

"X" = Jumper set (short) and "-" = jumper not set (open)

7.23.8. MFG Mode Selection (JP8)

The 2.0 mm pitch "MFG Mode Selection" jumper JP8 can be used to rewrite Intel ME firmware onto another version.

Figure 42: MFG Mode Selection JP8

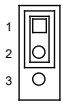


Table 49: Pin Assignment JP8

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal Operation (Default)
-	X	Enable MFG Mode

“X" = Jumper set (short) and “-" = jumper not set (open)

7.23.9. Clear CMOS Selection (JP9)

The 2.0 mm pitch "Clear COMS Selection" jumper JP9 can be used to reset the Real Time Clock (RTC) and drain RTC well.

The jumper has one position: Pin 1-2 mounted (default position) and Pin 2-3 mounted. More information on setting the "Clear CMOS Selection" jumper can be found in the following table.

Figure 43: Clear CMOS Selection JP9

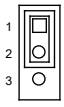


Table 50: Pin Assignment JP9

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal Operation (default position)
-	X	Clear CMOS (board does not boot with the jumper in this position)

“X" = Jumper set (short) and “-" = jumper not set (open)

Do not leave the jumper in position 2-3, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

8/ BIOS

8.1. Starting the uEFI BIOS

The 3.5"-SBC-RPL is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the 3.5"-SBC-RPL.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The 3.5"-SBC-RPL uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 51: Hotkeys Table

Signal	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the uEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows select major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
<↑> or <↓>	The <Up/Down> arrows select fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<RERURN>	The <RETURN> key executes a command or select a submenu.

8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Chipset
- Security
- Boot
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

Table 52: Main Setup Menu Sub-Screens and Functions

Function	Description
Product Information	Read only field. Displays information about the product name
BIOS Information	Read only field. Displays information about the system BIOS
FSP Information	Read only field. Display information about the FSP
Processor Information	Read only field. Display information about the processor
Memory Information	Read only field. Displays information about the memory
PCH Information	Read only field. Display information about the PCH
ME Information	Read only field. Display information about Intel Management Engine (ME) firmware
System Language	Read only field. [English] only
Platform Information	Sub-screen to board information.
System Date	Set System Date
System Time	Set System Time

Figure 44: BIOS Main Menu Screen System Data and Time

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Product Information					
Product Name		3.5-SBC-RPL			
BIOS Information					
BIOS Vendor		American Megatrends			
Core Version		5.32			
Compliancy		UEFI 2.9; PI 1.7			
Kontron BIOS Version		RPLUVEXR.113 (x64)			
Access Level		Administrator			
FSP Information					
FSP Version		0C.01.DE.40			
RC Version		0C.00.DE.40			
Build Date					
FSP Mode		Dispatch Mode			
Processor Information					
Name		Raptor Lake ULT			
Type		13th Gen Intel® Core™ i5-1345URE			
Speed		1400 MHz			
ID		0xB06A3			
Stepping		Q0			
Package		Not Implemented Yet			
Number of Efficient-cores		8 Core(s) / 8 Thread(s)			
Microcode Revision		4121			
GT Info		0xA721			
IGFX GOP Version		21.0.1065			
Memory RC Version		0.0.4.224			
Total Memory		8192 MB			
Memory Frequency		5200 MHz			
PCH Information					
Name		PCH-P			
PCH SKU		RPL-P: Industrial SKU			
Stepping		A1			
Chipset Init Base Revision		2			
Chipset Init OEM Revision		0			
Package		Not Implemented Yet			
TXT Capability of Platform / PCH		Supported			
Production Type		Production			

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Dual Output Fast Read Support		Supported			
Read ID / Status Clock Freq		50 MHz			
Write and Erase Clock Freq		50 MHz			
Fast Read Clock Freq		50 MHz			
Fast Read Support		Supported			
Number of Components		1 Component			
SPI Component 0 Density		32 MB			
eSPI Flash Sharing Mode		G3			
EC PECI Mode		Legacy PECI Mode			
ME FW Version		16.1.30.2307		→ ←: Select Screen	
ME Firmware SKU		Corporate SKU		↑ ↓: Select Item	
PMC FW Version		160.1.0.1030		Enter: Select	
				+/-: Change Opt.	
System Language		[English]		F1: General Help	
> Platform Information				F2: Previous Values	
				F3: Optimized Defaults	
System Date		[Tue 03/18/2025]		F4: Save & Exit	
System Time		[17:44:30]		ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

Feature	Option	Description
System Date	[dd/mm/yyyy]	Set the Date. Use Tab to switch between Data elements.
System Time	[hh:mm:ss]	Set the Time. Use Tab to switch between Time elements.

Figure 45: BIOS Main Menu Screen – Platform Information

Aptio Setup – AMI		
Main		
Product Information		
Product Name	3.5-SBC-RPL	
Serial #	Default String	
UUID	00020003-0004-0005-0006-000700080009	
KSC Information		
Controller	KSC Main Controller	
Operating Mode	Normal	
Board Name	3.5-RPL	
Platform ID	000C	→←: Select Screen
KSC SW Spec. Version	1.20	↑ ↓: Select Item
BIOS Protocol Version	2.3.1	Enter: Select
BIOS SW Spec. Version	1.18	+/-: Change Opt.
Core Firmware Version	1.4.1 Release	F1: General Help
Board Firmware Version	1.0.0 Release	F2: Previous Values
SCM Info	DB-8C-26-E2	F3: Optimized Defaults
		F4: Save & Exit
Boot Counter	N/A	ESC: Exit
Version 2.22.1293 Copyright (C) 2025 AMI		

8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- cTDP, IBECC, Compliance Test, Audio, Power, ME FW Image & AMT BIOS Features Configuration
- Display Configuration
- Trusted Computing
- ACPI Settings
- Miscellaneous
- MEBx
- H/W Monitor
- S5 RTC Wake Settings
- Serial Port Console Redirection
- SIO Configuration
- USB Configuration
- Network Stack Configuration
- NVMe Configuration
- CH7513A Configurations
- F81435 Configurations
- Driver Health

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 46: BIOS Advanced Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Configurable TDP Boot Mode			[15W]		
In-Band ECC Support			[Disabled]		
Compliance Test Mode			[Disabled]		
HD Audio			[Enabled]		
Power Mode Selection			[ATX Mode]		
Restore AC Power Loss			[Power Off]		
Power Saving Mode			[Disabled]		
ME FW Image Re-Flash			[Disabled]		
Unconfigure ME			[Disabled]		
AMT BIOS Features			[Disabled]		
> Display Configuration					
> Trusted Computing					
> ACPI Settings					
> Miscellaneous					
> MEBx					
> H/W Monitor					
> S5 RTC Wake Settings					
> Serial Port Console Redirection					
> SIO Configuration					
> USB Configuration					
> Network Stack Configuration					
> NVMe Configuration				→ ←: Select Screen	
> CH7513A Configurations				↑ ↓: Select Item	
> F81435 Configurations				Enter: Select	
				+/-: Change Opt.	
> RAM Disk Configuration*				F1: General Help	
> Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:02:A2*				F2: Previous Values	
> Intel® Ethernet Controller I226-IT – C0:EA:C3:D2:02:A3*				F3: Optimized Defaults	
				F4: Save & Exit	
> Driver Health				ESC: Exit	
Version 2.22.1293 Copyright (C) 2025 AMI					

* These sub-screen links have no function.

Feature	Option	Description
Configurable TDP Boot Mode	[15W], [9W]	Configurable Processor Base Power (cTDP) Mode as Nominal / Level 1 / Level 2 / Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
In-Band ECC Support	[Disabled], [Enabled]	Enable / Disable In-Band ECC. Will be enabled if memory has symmetric configuration
Compliance Test Mode	[Disabled], [Enabled]	Enable when using Compliance Load Board

Feature	Option	Description
HD Audio	[Disabled], [Enabled]	Control Detection of the HD-Audio device. [Disabled] = HDA will be unconditionally disabled. [Enabled] = HDA will be unconditionally enabled.
Power Mode Selection	[ATX Mode]	Read only item.
Restore AC Power Loss	[Power Off], [Last State]	Choose options for restoring AC power loss
Power Saving Mode	[Disabled], [Enabled]	Enable / Disable power saving mode
ME FW Image Re-Flash	[Disabled], [Enabled]	Enable / Disable ME FW Image Re-Flash function.
Unconfigure ME	[Disabled], [Enabled]	Unconfigure ME with resetting MEBx password to default on next boot.
AMT BIOS Features	[Disabled], [Enabled]	When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW.

Figure 47: BIOS Advanced Menu - Display Configuration

Aptio Setup – AMI		
Advanced		
Display Configuration		
Primary Display	[IGFX]	→←: Select Screen
Internal Graphics	[Enabled]	↑ ↓: Select Item
Aperture Size	[256MB]	Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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Feature	Option	Description
Primary Display	[Auto], [IGFX], [PEG Slot], [PCH PCI]	Select which of IGFX / PEG Graphics device should be Primary Display.
Internal Graphics	[Enabled]	Read only item
Aperture Size	[128MB], [256MB], [512MB], [1024MB]	Select the Aperture Size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting > 2048MB aperture. To use this feature, please disable CSM Support.

Figure 48: BIOS Advanced Menu - Trusted Computing

Aptio Setup – AMI		
Advanced		
TPM 2.0 Device Found		
Firmware Version:	16.13	
Vendor:	IFX	
Security Device Support	[Enabled]	
Active PCR banks*	SHA256	
Available PCR banks*	SHA256, SHA384	
SHA256 PCR Bank*	[Enabled]	
SHA384 PCR Bank*	[Disabled]	→←: Select Screen
		↑ ↓: Select Item
Pending operation*	[None]	Enter: Select
Platform Hierarchy*	[Enabled]	+/-: Change Opt.
Storage Hierarchy*	[Enabled]	F1: General Help
Endorsement Hierarchy*	[Enabled]	F2: Previous Values
Physical Presence Spec Version*	[1.3]	F3: Optimized Defaults
TPM 2.0 Interface Type*	[TIS]	F4: Save & Exit
Device Select*	[Auto]	ESC: Exit
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* These items appear only when enabling Security Device Support.

Feature	Option	Description
Security Device Support	[Disabled], [Enabled]	Enable or Disable BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
SHA256 PCR Bank	[Disabled], [Enabled]	Enable or Disable SHA256 PCR Bank
SHA384 PCR Bank	[Disabled], [Enabled]	Enable or Disable SHA384 PCR Bank
Pending operation	[None], [TPM Clear]	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	[Disabled], [Enabled]	Enable or Disable Platform Hierarchy
Storage Hierarchy	[Disabled], [Enabled]	Enable or Disable Storage Hierarchy
Endorsement Hierarchy	[Disabled], [Enabled]	Enable or Disable Endorsement Hierarchy
Physical Presence Spec Version	[1.2], [1.3]	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
TPM 2.0 Interface Type	[TIS]	Read only item

Feature	Option	Description
Device Select	[TPM 1.2], [TPM 2.0], [Auto]	TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.

Figure 49: BIOS Advanced Menu – ACPI Settings

Aptio Setup – AMI		
Advanced		
ACPI Settings		
Enable ACPI Auto Configuration	[Disabled]	→←: Select Screen ↑ ↓: Select Item
Enable Hibernation*	[Enabled]	Enter: Select
ACPI Sleep State*	[S3 (Suspend to RAM)]	+/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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* These items appear only when disabling Enable ACPI Auto Configuration.

Feature	Option	Description
Enable ACPI Auto Configuration	[Disabled], [Enabled]	Enables or Disables BIOS ACPI Auto Configuration.
Enable Hibernation	[Disabled], [Enabled]	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operating systems.
ACPI Sleep State	[Suspend Disabled], [S3 (Suspend to RAM)]	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

Figure 50: BIOS Advanced Menu – Miscellaneous

Aptio Setup – AMI		
Advanced		
Miscellaneous Configuration		
> Preset DIO in BIOS		
> Control KSC firmware		
> Update KSC firmware		
> Generic eSPI Decode Ranges		
> Watchdog		
Reset Button Behavior	[Chipset Reset]	
I2C Speed	[100 KHz]	→←: Select Screen
Onboard I2C Mode	[Multimaster]	↑ ↓: Select Item
Manufacturing mode	[Disabled]	Enter: Select
BIOS Test Mode	[Disabled]	+/-: Change Opt.
Last system reset through	[Power-on reset]	F1: General Help
	[Disabled]	F2: Previous Values
PCIe Wake		F3: Optimized Defaults
		F4: Save & Exit
Onboard EEPROM Write Protect	[WP Enabled]	ESC: Exit
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Feature	Option	Description
Reset Button Behavior	[Chipset Reset], [Power Cycle]	Select Reset Button Behavior: Chipset Reset & Power Cycle.
I2C Speed	[100 KHz], [400 KHz], [1 MHz]	Select I2C Bus Speed in KHz. For a default system 100 KHz should be an appropriate value.
Onboard I2C Mode	[Multimaster], [Busclear]	MultiMaster / BusClear
Manufacturing mode	[Disabled]	Read only item
BIOS Test Mode	[Disabled]	Read only item
Last system reset through	[Power-on reset]	Read only item
PCIe Wake	[Disabled], [Enabled]	Set to enable or disable PCIe wake. This would affect features such as Wake 0/1 and Wake from Lan (WOL).
Onboard EEPROM Write Protect	[WP Disabled], [WP Enabled]	Set WP enable or disable the Onboard EEPROM Write Protect

Figure 51: BIOS Advanced Menu – Miscellaneous – Preset DIO in BIOS

Aptio Setup – AMI
Advanced

Aptio Setup – AMI		
Advanced		
Allows to preset GPIOs during BIOS startup.		
GPIO OS usable	[GPIO 0 – GPIO 7]	
Control DIO in BIOS	[Disabled]	
DIO #0*	[Skip]	
Output level*(1)	[Low]	
DIO #1*	[Skip]	
Output level*(1)	[Low]	
DIO #2*	[Skip]	
Output level*(1)	[Low]	
DIO #3*	[Skip]	
Output level*(1)	[Low]	→←: Select Screen
DIO #4*	[Skip]	↑ ↓: Select Item
Output level*(1)	[Low]	Enter: Select
DIO #5*	[Skip]	+/-: Change Opt.
Output level*(1)	[Low]	F1: General Help
DIO #6*	[Skip]	F2: Previous Values
Output level*(1)	[Low]	F3: Optimized Defaults
DIO #7*	[Skip]	F4: Save & Exit
Output level*(1)	[Low]	ESC: Exit
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* These items appear only when enabling Control DIO in BIOS.

(1) This item appears only when selecting Output for DIO #0/1/2/3/4/5/6/7 respectively.

Feature	Option	Description
GPIO OS usable	[All available GPIO], [GPIO 0 – GPIO 7]	Set the GPIO OS usable
Control DIO in BIOS	[Disabled], [Enabled]	Enables or disables DIO GPIO control in BIOS. If set to 'disabled' then the GPIOs are not touched by BIOS.
DIO #0..7	[Input], [Output], [Skip]	Determine the type of the DIO configuration. If this is set to 'Skip' then this GPIO will be left untouched.
Output level	[Low], [High]	Set the level of a DIO pin

Figure 52: BIOS Advanced Menu – Miscellaneous – Control KSC firmware

Aptio Setup – AMI	
Advanced	
Allows to control KSC firmware related settings.	

Aptio Setup – AMI		
Advanced		
Lock FW update access	[Enabled]	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
> KSC OTP area control		
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Feature	Option	Description
Lock FW update access	[Disabled], [Enabled]	Locks access to KSC firmware area during runtime.

Figure 53: BIOS Advanced Menu – Miscellaneous – Control KSC firmware – KSC OTP area control

Aptio Setup – AMI		
Advanced		
Allows to control KSC OTP area related settings.		
KSC OTP access lock	[Enabled]	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Feature	Option	Description
KSC OTP access lock	[Enabled]	Read only item

Figure 54: BIOS Advanced Menu – Miscellaneous – Update KSC firmware

Aptio Setup – AMI		
Advanced		
Allows to update KSC firmware from BIOS.		
Auto update KSC FW	[Disabled]	→←: Select Screen

Aptio Setup – AMI	
Advanced	
	↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Feature	Option	Description
Auto update KSC FW	[Disabled], [Enabled]	Updates KSC firmware to BIOS internal version (best known config) on next system start. To update FW set item to 'Enabled' and exit the setup using 'Save changes and exit'.

Figure 55: BIOS Advanced Menu – Miscellaneous – Generic eSPI Decode Ranges

Aptio Setup – AMI		
Advanced		
Generic eSPI Decode Ranges		
Generic LPC via eSPI Decode 1	[Disabled]	→ ←: Select Screen
Base Address*	100	↑ ↓: Select Item
Length*	8	Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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* These items appear only when enabling Generic LPC via eSPI Decode 1.

Feature	Option	Description
Generic LPC via eSPI Decode 1	[Disabled], [Enabled]	Enable generic LPC via eSPI decode range.
Base Address	Value input	Base address of the generic decode range. Valid between 0100h – FFF0h. Must be 8-byte aligned. Please note that it also has to be length-aligned.
Length	Value input	Length of the generic decode range in hexadecimal notation. Valid between 0008h – 0100h. Must be multiple of 8h.

Figure 56: BIOS Advanced Menu – Miscellaneous – Watchdog

Aptio Setup – AMI		
Advanced		
Watchdog Configuration.		
Auto-reload	[Disabled]	
Global Lock	[Disabled]	
WDT Strobe	[Disabled]	
Stage 1 Mode	[Disabled]	
Assert WDT Signal (1)	[Disabled]	
Stage 1 Timeout (2)	[1m]	→←: Select Screen
		↑ ↓: Select Item
Stage 2 Mode (3)	[Delay]	Enter: Select
Assert WDT Signal (1)	[Disabled]	+/-: Change Opt.
Stage 2 Timeout (2)	[1m]	F1: General Help
		F2: Previous Values
Stage 3 Mode (3)	[Delay]	F3: Optimized Defaults
Assert WDT Signal (1)	[Disabled]	F4: Save & Exit
Stage 3 Timeout (2)	[1m]	ESC: Exit
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(1) This item appears only when selecting Reset or Delay for Stage 1/2/3 Mode.

(2) This item appears only when selecting Reset, Delay or WDT Signal only for Stage 1/2/3 Mode.

(3) This item appears only when selecting Delay for Stange N-1 Mode.

Feature	Option	Description
Auto-reload	[Disabled], [Enabled]	Enable automatic reload of watchdog timers on timeout.
Global Lock	[Disabled], [Enabled]	If set to enabled, all Watchdog registers (except WD_KICK) become read only until the board is reset.
WDT Strobe	[Disabled], [Enabled]	Enable / disable WDT Strobe input.
Stage 1/2/3 Mode	[Disabled], [Reset], [Delay], [WDT Signal only]	Select Action for this Watchdog stage
Assert WDT Signal	[Disabled], [Enabled]	Enable / disable assertion of WDT signal to baseboard on stage timeout.
Stage 1/2/3 Timeout	[1m], [3m], [10m], [30m]	Select Timeout value for this Watchdog stage

Figure 57: BIOS Advanced Menu – MEBx*

Aptio Setup – AMI	
Advanced	
Intel® ME Password	
	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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* This sub-screen is available only when enabling AMT BIOS Features.

Feature	Option	Description
Intel ME Password	Password input	Default password "admin".

Follow the instructions to configure the settings after entering the password.

Figure 58: BIOS Advanced Menu – H/W Monitor

Aptio Setup – AMI		
Advanced		
KSC based H/W Monitor		
Temperature sensors:		
#1: CPU Temp	: + 55.9 C	
#2: PCH Temp	: + 50.0 C	
#3: SYSTEM Temp	: + 48.1 C	
Voltage sensors:		
#1: V_IN	: 24.2 V	
#2: 12V_S0	: 12.2 V	
#3: 5V_S0	: 5.2 V	
#4: 3V3_S0	: 3.4 V	
#5: 3V_BAT	: 2.8 V	
Fan speed & control:		
#1: CPU Fan	: 0 RPM	
Fan Control	[Auto]	
Signal Filter Control*#	[Auto]	→←: Select Screen
Signal Filter*#(1)	Enabled	↑ ↓: Select Item
Fan Pulse*#	[Auto]	Enter: Select
Fan Pulse*#(2)	: 2	+/-: Change Opt.
Fan Speed Control*#	[Auto]	F1: General Help
Fan Speed Control*#(3)	Normal	F2: Previous Values
Fan Speed#	100	F3: Optimized Defaults
Reference Temperature*	[All Temperatures]	F4: Save & Exit
> Fan #1 Trip Point Table*		ESC: Exit
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* These items appear when selecting Auto for Fan Control.

These items appear when selecting Manual for Fan Control.

(1) This item appears only when selecting Auto for Signal Filter Control.

(2) This item appears only when selecting Auto for Fan Pulse.

(3) This item appears only when selecting Auto for Fan Speed Control.

Feature	Option	Description
Fan Control	[Disabled], [Manual], [Auto]	Set fan control mode. 'Disabled' will disable the control circuit and stops the fan.
Signal Filter Control	[Disabled], [Enabled], [Auto]	Enable / Disable Fab Tacho Signal Filter. [Auto] = Setting from KSC

Feature	Option	Description
Fan Pulse	[Auto], [1], [2], [3], [4], [5], [6], [7], [8]	Number of pulses the fan produces during one revolution. Range: 1 - 8
Fan Speed Control	[Normal], [Reverse], [Auto]	Set fan speed control method. [Auto] = Setting from KSC [Normal] = Signal has normal behaviour [Reverse] = Signal has reversed behaviour
Fan Speed	Value input	Manual fan speed in %
Reference Temperature	[#1: CPU Temp], [#2: PCH Temp], [#3: SYSTEM Temp], [All Temperatures]	Determines the temperature source which is used for automatic fan control

Figure 59: BIOS Advanced Menu – H/W Monitor – Fan #1 Trip Point Table

Aptio Setup – AMI		
Advanced		
Fan #1 Automode	[Internal table]	
Fan Trip Point 1*	50	
Fan Hysteresis 1*	50	
Fan TP Speed 1*	54	
Fan Trip Point 2*	60	
Fan Hysteresis 2*	55	
Fan TP Speed 2*	58	→←: Select Screen
		↑ ↓: Select Item
Fan Trip Point 3*	70	Enter: Select
Fan Hysteresis 3*	61	+/-: Change Opt.
Fan TP Speed 3*	82	F1: General Help
		F2: Previous Values
Fan Trip Point 4*	80	F3: Optimized Defaults
Fan Hysteresis 4*	71	F4: Save & Exit
Fan TP Speed 4*	100	ESC: Exit
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* These items appear only when selecting User table for Fan #1 Automode.

Feature	Option	Description
Fan #1 Automode	[Internal table], [User table]	Chooses between internal table and user table for automatic fan control.
Fan Trip Point 1/2/3/4	Value input	Set trip point in deg Celsius
Fan Hysteresis 1/2/3/4	Value input	Set hysteresis in deg Celsius
Fan TP Speed	Value input	Set trip point speed in % between 0 (stop) and 100 (full).

Feature	Option	Description
1/2/3/4		

Figure 60: BIOS Advanced Menu – S5 RTC Wake Settings

Aptio Setup – AMI		
Advanced		
Wake system from S5	[Disabled]	
Wake up hour [1]	0	
Wake up minute [1]	0	→←: Select Screen
Wake up second [1]	0	↑ ↓: Select Item
Wake up minute increase [2]	1	Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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[1] These items appear only when selecting Fixed Time for Wake system from S5.

[2] This item appears only when selecting Dynamic Time for Wake system from S5.

Feature	Option	Description
Wake system from S5	[Disabled], [Fixed Time], [Dynamic Time]	Enable or disable System wake on alarm event. Select Fixed Time, system will wake on the hr::min::sec specified. Select Dynamic Time, system will wake on the current time + Increase minute(s).
Wake up hour	Value input	Select 0 – 23 For example, enter 3 for 3 am and 15 for 3 pm.
Wake up minute	Value input	Select 0 – 59 for Minute
Wake up second	Value input	Select 0 – 59 for Second
Wake up minute increase	Value input	1 - 5

Figure 61: BIOS Advanced Menu – Serial Port Console Redirection

Aptio Setup – AMI		
Advanced		
COM0		
Console Redirection	[Disabled]	
> Console Redirection Settings*		
COM1		
Console Redirection	[Disabled]	
> Console Redirection Settings*		→ ←: Select Screen
		↑ ↓: Select Item
Legacy Console Redirection		Enter: Select
> Legacy Console Redirection Settings#		+/-: Change Opt.
		F1: General Help
Serial Port for Out-of-Band Management / Windows Emergency		F2: Previous Values
Management Services (EMS)		F3: Optimized Defaults
Console Redirection EMS	[Disabled]	F4: Save & Exit
> Console Redirection Settings*		ESC: Exit
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* These items activate only when enabling Console Redirection (EMS).

This sub-screen link has no funtion.

Feature	Option	Description
Console Redirection (EMS)	[Disabled], [Enabled]	Console Redirection Enable or Disable.

Figure 62: BIOS Advanced Menu – Serial Port Console Redirection – COM0/1 Console Redirection Settings

Aptio Setup – AMI		
Advanced		
COM0/1		
Console Redirection Settings		
Terminal Type	[ANSI]	
Bits per second	[115200]	→ ←: Select Screen
Data Bits	[8]	↑ ↓: Select Item
Parity	[None]	Enter: Select
Stop Bits	[1]	+/-: Change Opt.
Flow Control	[None]	F1: General Help
VT-UTF8 Combo Key Support	[Enabled]	F2: Previous Values
Recorder Mode	[Disabled]	F3: Optimized Defaults
Resolution 100x31	[Disabled]	F4: Save & Exit
Putty KeyPad	[VT100]	ESC: Exit

Aptio Setup – AMI
Advanced
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Feature	Option	Description
Terminal Type	[VT100], [VT100Plus], [VT-UTF8], [ANSI]	Emulation: [ANSI]: Extended ASCII char set. [VT100]: ASCII char set. [VT100Plus]: Extends VT100 to support color, function keys, etc. [VT-UTF8]: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
Bits per second	[9600], [19200], [38400], [57600], [115200], [230400], [460800], [921600]	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data Bits	[7], [8]	Data Bits
Parity	[None], [Even], [Odd], [Mark], [Space]	A parity bit can be sent with the data bits to detect some transmission errors. [Even]: parity bit is 0 if the num of 1's in the data bits is even. [Odd]: parity bit is 0 if num of 1's in the data bits is odd. [Mark]: parity bit is always 1. [Space]: Parity bit is always 0. Mark and Space Parity do not allow for error detection. They can be used as an additional data bit.
Stop Bits	[1], [2]	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	[None], [Hardware RTS/CTS]	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start / stop signals.
VT-UTF8 Combo Key Support	[Disabled], [Enabled]	Enable VT-UTF8 Combination Key Support for ANSI / VT100 terminals
Recorder Mode	[Disabled], [Enabled]	With this mode enabled only text will be sent. This is to capture Terminal data.
Resolution 100x31	[Disabled], [Enabled]	Enables or disables extended terminal resolution
Putty KeyPad	[VT100], [LINUX], [XTERMR6], [SCO], [ESCN],	Select FunctionKey and KeyPad on Putty.

Feature	Option	Description
	[VT400]	

Figure 63: BIOS Advanced Menu – Serial Port Console Redirection – Console Redirection EMS Settings

Aptio Setup – AMI		
Advanced		
Out-of-Band Mgmt Port	[COM0]	
Terminal Type EMS	[VT-UTF8]	
Bits per second EMS	[115200]	→←: Select Screen
Flow Control EMS	[None]	↑ ↓: Select Item
Data Bits EMS	8	Enter: Select
Parity EMS	None	+/-: Change Opt.
Stop Bits EMS	1	F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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Feature	Option	Description
Out-of-Band Mgmt Port	[COM0], [COM1]	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
Terminal Type EMS	[VT100], [VT100Plus], [VT-UTF8], [ANSI]	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type / Emulation.
Bits per second EMS	[9600], [19200], [57600], [115200], [230400], [460800], [921600]	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Flow Control EMS	[None], [Hardware RTS/CTS], [Software Xon/Xoff]	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start / stop signals.

Figure 64: BIOS Advanced Menu – SIO Configuration

Aptio Setup – AMI	
Advanced	
AMI SIO Driver Version: A5.19.00	
Super IO Chip Logical Devices(s) Configuration > [*Active*] Serial Port 0 > [*Active*] Serial Port 1 WARNING: Logical Devices state on the left side of the control, reflects the current Logical Device state. Changes made during Setup Session will be shown after you restart the system.	→ ←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 65: BIOS Advanced Menu – SIO Configuration – [*Active*] Serial Port 0

Aptio Setup – AMI		
Advanced		
Serial Port 0 Configuration		
Use This Device	[Enabled]	→ ←: Select Screen ↑ ↓: Select Item
Logical Device Settings:* Current: IO=3F8h; IRQ=4;*		Enter: Select +/-: Change Opt. F1: General Help
Possible:*	[Use Automatic Settings]	F2: Previous Values F3: Optimized Defaults
WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		F4: Save & Exit ESC: Exit
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* These items appear only when enabling Use This Device.

Feature	Option	Description
Use This Device	[Disabled], [Enabled]	Enables or Disables this Logical Device.
Possible:	[Use Automatic Settings], [IO=3F8h; IRQ=4;], [IO=3F8h; IRQ=4;], [IO=2F8h; IRQ=3;]	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Figure 66: BIOS Advanced Menu – SIO Configuration – [*Active*] Serial Port 1

Aptio Setup – AMI		
Advanced		
Serial Port 1 Configuration		
Use This Device	[Enabled]	→ ←: Select Screen ↑ ↓: Select Item
Logical Device Settings:*		Enter: Select
Current: IO=2F8h; IRQ=3;*		+/-: Change Opt.
Possible:*	[Use Automatic Settings]	F1: General Help F2: Previous Values F3: Optimized Defaults
WARNING: Disabling SIO Logical Devices may have unwanted side effects. PROCEED WITH CAUTION.		F4: Save & Exit ESC: Exit
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* These items appear only when enabling Use This Device.

Feature	Option	Description
Use This Device	[Disabled], [Enabled]	Enables or Disables this Logical Device.
Possible:	[Use Automatic Settings], [IO=2F8h; IRQ=3;], [IO=2F8h; IRQ=3;], [IO=3F8h; IRQ=4;]	Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.

Figure 67: BIOS Advanced Menu – USB Configuration

Aptio Setup – AMI		
Advanced		
USB Configuration USB Module Version	34	
USB Controllers: 1 XHCIs USB Devices: 1 Keyboard		
Legacy USB Support	[Enabled]	→←: Select Screen
XHCI Hand-off	[Disabled]	↑ ↓: Select Item
USB Mass Storage Driver Support	[Enabled]	Enter: Select
		+/-: Change Opt.
USB hardware delays and time-outs:		F1: General Help
USB transfer time-out	[20 sec]	F2: Previous Values
Device reset time-out	[20 sec]	F3: Optimized Defaults
Device power-up delay	[Auto]	F4: Save & Exit
Device power-up delay in seconds*	5	ESC: Exit
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* This item appears only when selecting Manual for Device power-up delay in seconds.

Feature	Option	Description
Legacy USB Support	[Enabled], [Disabled], [Auto]	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI Hand-off	[Enabled], [Disabled]	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	[Disabled], [Enabled]	Enable / Disable USB Mass Storage Driver Support.
USB transfer time-out	[1 sec], [5 sec], [10 sec], [20 sec]	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	[10 sec], [20 sec], [30 sec], [40 sec]	USB mass storage device Start Unit command time-out.
Device power-up delay	[Auto], [Manual]	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub

Feature	Option	Description
		descriptor.
Device power-up delay in seconds	Value input	Delay range is 1..40 seconds, in one second increments

Figure 68: BIOS Advanced Menu – Network Stack Configuration

Aptio Setup – AMI		
Advanced		
Network Stack	[Disabled]	
IPv4 PXE Support*	[Disabled]	
IPv4 HTTP Support*	[Disabled]	→←: Select Screen
IPv6 PXE Support*	[Disabled]	↑ ↓: Select Item
IPv6 HTTP Support*	[Disabled]	Enter: Select
PXE boot wait time*	0	+/-: Change Opt.
Media detect count*	1	F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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* Thess items appear only when enabling Network Stack.

Feature	Option	Description
Network Stack	[Disabled], [Enabled]	Enable / Disable UEFI Network Stack
IPv4 PXE Support	[Disabled], [Enabled]	Enable / Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support	[Disabled], [Enabled]	Enable / Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support	[Disabled], [Enabled]	Enable / Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 HTTP Support	[Disabled], [Enabled]	Enable / Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time	Value input	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count	Value input	Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

Figure 69: BIOS Advanced Menu – NVMe Configuration

Aptio Setup – AMI		
Advanced		
NVMe Controller and Drive information		
Bus: 1 Dev: 0 Func: 0	TS128GMTE652T	→←: Select Screen
Nvme Size	128.0GB	↑ ↓: Select Item
		Enter: Select
		+/-: Change Opt.
		F1: General Help
		F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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Read only sub-screen

Figure 70: BIOS Advanced Menu – CH7513A Configurations

Aptio Setup – AMI		
Advanced		
CH7513A Configurations		
LFP Selection	[Disabled]	
LVDS ACPI Device (1)(2)	[Enabled]	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
LVDS Panel Type (1)	[1920x1080 24Bit 2CH]	
Backlight Source Selection (1)(2)	[Controlled by PCH]	
Panel Brightness (1)(2)*	100	
Panel PWM (1)(2)*	[Normal PWM]	
Panel PWM Frequency (1)(2)*	[200]	
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(1) These items appear when selection LVDS for LFP Selection.

(2) These items appear when selecting eDP for LFP Selection.

* These items appear only when selecting Controlled by EC for Backlight Source Selection.

Feature	Option	Description
LFP Selection	[Disabled], [LVDS], [eDP]	Select the LFP Configuration
LVDS ACPI Device	[Disabled], [Enabled]	Enabled / Disabled LVDS ACPI Device SMB0001
LVDS Panel Type	[CUSTOM], [1024x768 18Bit 1CH], [1024x768 24Bit 1CH], [1280x768 18Bit 1CH], [1280x800 18Bit 1CH], [1280x960 18Bit 1CH], [1280x1024 24Bit 2CH], [1366x768 18Bit 1CH], [1366x768 24Bit 1CH], [1440x900 24Bit 2CH], [1400x1050 24Bit 2CH], [1600x900 24Bit 2CH], [1680x1050 24Bit 2CH], [1600x1200 24Bit 2CH], [1920x1080 24Bit 2CH], [1920x1200 24Bit 2CH]	LVDS panel by selecting the appropriate setup item.
Backlight Source Selection	[Controlled by EC], [Controlled by PCH], [Controlled by Switch]	Set the backlight source Selection

Feature	Option	Description
Panel Brightness	Value input	Set panel brightness value controlled by EC. Range is between 0% – 100%
Panel PWM	[Normal PWM], [Inverted PWM]	Set panel PWM behavior
Panel PWM Frequency	[200], [1K], [5K], [10K], [20K], [30K], [40K]	Set panel PWM Frequency

Figure 71: BIOS Advanced Menu – F81435 Configurations

Aptio Setup – AMI		
Advanced		
F81435 Configurations		
COM1 Mode Selection	[RS-232]	→←: Select Screen
COM1 Transceiver	[Normal mode]	↑ ↓: Select Item
COM1 Internal Terminator Switch Control	[Terminator switch is disabled]	Enter: Select
COM1 External Terminator Switch Control	[Terminator switch is disabled]	+/-: Change Opt.
		F1: General Help
COM2 Mode Selection	[RS-232]	F2: Previous Values
COM2 Transceiver	[Normal mode]	F3: Optimized Defaults
COM2 Internal Terminator Switch Control	[Terminator switch is disabled]	F4: Save & Exit
COM2 External Terminator Switch Control	[Terminator switch is disabled]	ESC: Exit
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Feature	Option	Description
COM1/2 Mode Selection	[RS-422 Signal Master], [RS-232], [RS-485 with Auto Flow Control], [RS-422 Multi Master]	Mode selection for COM1/2
COM1/2 Transceiver	[Shutdown mode], [Normal mode]	Shutdown the Transceiver of COM1/2
COM1/2 Internal Terminator Switch Control	[Terminator switch is disabled], [Terminator switch is enabled]	Internal Terminator switch control for RS-422 / RS-485 of COM1/2
COM1/2 External Terminator Switch Control	[Terminator switch is disabled], [Terminator switch is enabled]	External Terminator switch control for RS-422 / RS-485 of COM1/2

Figure 72: BIOS Advanced Menu – Driver Health

Aptio Setup – AMI		
Advanced		
> Intel® 2.5G Ethernet Controller 0.10.06	Healthy	
> Intel® 2.5G Ethernet Controller 0.10.06	Healthy	
		→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 73: BIOS Advanced Menu – Driver Health – Intel® 2.5G Ethernet Controller 0.10.06

Aptio Setup – AMI		
Advanced		
Intel® Ethernet Controller I226-IT	Healthy	
Intel® Ethernet Controller I226-IT	Healthy	
		→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Read only

8.2.3. Chipset Setup Menu

The Chipset setup menu provides functions and a sub-screen for chipset configurations. The following sub-screen functions are included in the menu:

- System Agent (SA) Configuration
- PCH-IO Configuration

Figure 74: BIOS Chipset Setup Menu

Aptio Setup – AMI					
Main	**Advanced**	**Chipset**	**Security**	**Boot**	**Save & Exit**
> System Agent (SA) Configuration > PCH-IO Configuration					
				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Figure 75: BIOS Chipset Setup Menu – System Agent (SA) Configuration

Aptio Setup – AMI		
Chipset		
System Agent (SA) Configuration		
VT-d	Supported	→ ←: Select Screen
		↑ ↓: Select Item
> Graphics Configuration		Enter: Select
		+/-: Change Opt.
VT-d	[Enabled]	F1: General Help
Above 4GB MMIO BIOS assignment	[Enabled]	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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Feature	Option	Description
VT-d	[Enabled], [Disabled]	VT-d capability
Above 4GB MMIO BIOS assignment	[Enabled], [Disabled]	Enable / Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

Figure 76: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration

Aptio Setup – AMI		
Chipset		
Graphics Configuration		
Graphics Turbo IMON Current	31	
Skip Scaning of External Gfx Card	[Disabled]	
Select PCIE Card	[Auto]	
HG Delay After Power Enable	300	
HG Delay After Hold Reset	100	
> External Gfx Card Primary Display Configuration		
GTT Size	[8MB]	
PSMI SUPPORT	[Disabled]	
PSMI Region Size (1)	[32MB]	
DVMT Total Gfx Mem	[256M]	
Igfx Gsm2	[0GB]	
Intel Graphics Pei Display Peim	[Disabled]	
VDD Enable	[Enabled]	
Configure GT for use	[Enabled]	

Aptio Setup – AMI		
Chipset		
RC1p Support [2]	[Disabled]	→←: Select Screen
PAVP Enable	[Enabled]	↑ ↓: Select Item
Cdynmax Clamping Enable	[Disabled]	Enter: Select
Cd Clock Frequency	[Max CdClock freq based on Reference Clk]	+/-: Change Opt.
VBT Select	[eDP]	F1: General Help
Enable Display Audio Link in Pre-OS	[Disabled]	F2: Previous Values
IUER Button Enable	[Disabled]	F3: Optimized Defaults
> LCD Control		F4: Save & Exit
> Intel® Ultrabook Event Support		ESC: Exit
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[1] This item appears only when enabling PSMI SUPPORT.

[2] This item appears only when enabling Configure GT for use.

Feature	Option	Description
Graphics Turbo IMON Current	Value input	Graphics turbo IMON current values supported (14 - 31)
Skip Scaning of External Gfx Card	[Disabled], [Enabled]	If Enable, it will not scan for External Gfx Card on PEG and PCH PCIE Ports
Select PCIE Card	[Auto], [Elk Creek 4], [PEG Eval]	Select the card used on the platform [Auto]: Skip GPIO based Power Enable to dGPU [Elk Creek 4]: DGPU Power Enable = Active Low [PEG Eval]: DGPU Power Enable = Active High
HG Delay After Power Enable	Value input	Delay in milli-seconds after power enable
HG Delay After Hold Reset	Value input	Delay in milli-seconds after hold reset
GTT Size	[2MB], [4MB], [8MB]	Select the GTT Size
PSMI SUPPORT	[Disabled], [Enabled]	PSMI Enable / Disable
PSMI Region Size	[32MB], [288MB], [544MB], [800MB], [1024MB]	Select the PSMI Region Size: Range from 32MB to 1024MB
DVMT Total Gfx Mem	[128M], [256M], [MAX]	Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.
Igfx Gsm2	[0GB], [2GB], [4GB], [6GB], [8GB], [10GB], [12GB], [14GB], [16GB], [18GB], [20GB], [22GB], [24GB],	Graphics Stolen Memory 2

Feature	Option	Description
	[26GB], [28GB], [30GB], [32GB]	
Intel Graphics Pei Display Peim	[Enabled], [Disabled]	Enable / Disable Pei (Early) Display
VDD Enable	[Disabled], [Enabled]	Enable / Disable forcing of VDD in the BIOS
Configure GT for use	[Enabled], [Disabled]	Enable / Disable GT configuration in BIOS
RC1p Support	[Enabled], [Disabled]	Enable / Disable RC1p support. If RC1p is enabled, send a RC1p frequency request to PMA based other conditions being met
PAVP Enable	[Enabled], [Disabled]	Enable / Disable PAVP
Cdynmax Clamping Enable	[Enabled], [Disabled]	Enable / Disable Cdynmax Clamping
Cd Clock Frequency	[192 Mhz], [307.2 Mhz], [556.8 Mhz], [652.8 Mhz], [Max CdClock freq based on Reference Clk]	Select the highest Cd Clock frequency supported by the platform
VBT Select	[eDP], [MIPI], [ADLP/RPLP RVP DDR5], [ADLP RVP DDR4], [RPLP CRB]	Select VBT for GOP Driver Select VBT to MIPI if any of the Display has MIPI
Enable Display Audio Link in Pre-OS	[Disabled], [Enabled]	[Enabled]: Display Audio Link will be enabled in Pre-OS. [Disabled]: Display Audio Link will be disabled in Pre-OS.
IUER Button Enable	[Disabled], [Enabled]	Enable / Disable IUER Button Functionality

Figure 77: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – External Gfx Card Primary Display Configuration

Aptio Setup – AMI	
Chipset	
External Gfx Card Primary Display Configuration	
	→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values

Aptio Setup – AMI	
Chipset	
	F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Figure 78: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – LCD Control

Aptio Setup – AMI		
Chipset		
LCD Control		
LCD Panel Type	[VBIOS Default]	→←: Select Screen
Panel Scaling	[Auto]	↑ ↓: Select Item
Backlight Control	[PWM Normal]	Enter: Select
Active LFP	[eDP Port-A]	+/-: Change Opt.
Panel Color Depth	[18 Bit]	F1: General Help
Backlight Brightness	255	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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Feature	Option	Description
LCD Panel Type	[VBIOS Default], [640x480 LVDS], [800x600 LVDS], [1024x768 LVDS], [1280x1024 LVDS], [1400x1050 LVDS1], [1400x1050 LVDS2], [1600x1200 LVDS], [1280x768 LVDS], [1680x1050 LVDS], [1920x1200 LVDS], [1600x900 LVDS], [1280x800 LVDS], [1280x600 LVDS], [2048x1536 LVDS], [1366x768 LVDS]	Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
Panel Scaling	[Auto], [Off], [Force Scaling]	Select the LCD panel scaling option used by the Internal Graphics Device.
Backlight Control	[PWM Inverted], [PWM Normal]	Back Light Control Setting

Feature	Option	Description
Active LFP	[No eDP], [eDP Port-A]	Select the Active LFP Configuration. [No LVDS]: VBIOS does not enable LVDS. [Int-LVDS]: VBIOS enables LVDS driver by Integrated encoder. [SDVO LVDS]: VBIOS enables LVDS driver by SDVO encoder. [eDP Port-A]: LFP Driven by Int-DisplayPort encoder from Port-A. [eDP Port-D]: LFP Driven by Int-DisplayPort encoder from Port-D (through PCH).
Panel Color Depth	[18 Bit], [24 Bit]	Select the LFP Panel Color Depth
Backlight Brightness	Value input	Set VBIOS Brightness. Range: 0 – 255.

Figure 79: BIOS Chipset Setup Menu – System Agent (SA) Configuration – Graphics Configuration – Intel® Ultrabook Event Support

Aptio Setup – AMI		
Chipset		
Intel® Ultrabook Event Support		
IUER Slate Enable	[Disabled]	→←: Select Screen
Slate Mode boot value (1)	[Laptop Mode]	↑ ↓: Select Item
Slate Mode on S3 and S4 resume (1)	[No change]	Enter: Select
IUER Dock Enable	[Disabled]	+/-: Change Opt.
Dock Mode boot value (2)	[Undocked]	F1: General Help
Dock Mode upon S3 and S4 resume (2)	[No change]	F2: Previous Values
		F3: Optimized Defaults
		F4: Save & Exit
		ESC: Exit
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(1) These items appear only when enabling IUER Slate Enable.

(2) These items appear only when enabling IUER Dock Enable.

Feature	Option	Description
IUER Slate Enable	[Disabled], [Enabled]	Enable / Disable IUER Slate Functionality
Slate Mode boot value	[Slate Mode], [Laptop Mode]	Choose Slate or Laptop as boot mode.
Slate Mode on S3 and S4 resume	[No change], [Toggle]	Keep it the same as Sx entry or toggle it.
IUER Dock Enable	[Disabled], [Enabled]	Enable / Disable IUER Dock Functionality
Dock Mode boot value	[Undocked], [Docked]	Choose Docked or Undocked as boot mode.
Dock Mode upon S3	[No change],	Keep it the same as Sx entry or toggle it.

Feature	Option	Description
and S4 resume	[Toggle]	

Figure 80: BIOS Chipset Setup Menu – PCH-IO Configuration

Aptio Setup – AMI		
Chipset		
PCH-IO Configuration		
> PCI Express Configuration		
> SATA Configuration		→←: Select Screen
> USB Configuration		↑ ↓: Select Item
		Enter: Select
> TSN GBE Configuration*		+/-: Change Opt.
		F1: General Help
PCH LAN Controller	No GbE Region	F2: Previous Values
Port 80h Redirection	[LPC Bus]	F3: Optimized Defaults
Enhance Port 80h LPC Decoding#	[Enabled]	F4: Save & Exit
Compatible Revision ID	[Disabled]	ESC: Exit
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* This sub-screen link has no function.

This item activates only when selecting LPC Bus for Port 80h Redirection.

Feature	Option	Description
Port 80h Redirection	[LPC Bus], [PCIE Bus]	Control where the Port 80h cycles are sent.
Enhance Port 80h LPC Decoding	[Disabled], [Enabled]	Support the word / dword decoding of port 80h behind LPC
Compatible Revision ID	[Disabled]	Read only item

Figure 81: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration

Aptio Setup – AMI		
Chipset		
PCI Express Configuration		
DMI Link ASPM Control	[Auto]	
Port8xh Decode	[Disabled]	
Port8xh Decode Port#*	0	
PCIe function swap	[Enabled]	
PCH PCIE Clock Gating	[Disabled]	
PCH PCIE Power Gating	[Disabled]	
> PCIe EQ settings		
PCI Express Root Port 1	Lane configured as USB / SATA / UFS	
PCI Express Root Port 2	Lane configured as USB / SATA / UFS	
PCI Express Root Port 3	Lane configured as USB / SATA / UFS	

Aptio Setup – AMI		
Chipset		
PCI Express Root Port 4	Lane configured as USB / SATA / UFS	
> PCI Express Root Port 5		
PCI Express Root Port 6	Shadowed by x2/x4 port	→←: Select Screen
> PCI Express Root Port 7		↑ ↓: Select Item
> PCI Express Root Port 8		Enter: Select
> PCI Express Root Port 9		+/-: Change Opt.
> PCI Express Root Port 10		F1: General Help
PCI Express Root Port 11	Lane configured as USB / SATA / UFS	F2: Previous Values
> PCI Express Root Port 12		F3: Optimized Defaults
		F4: Save & Exit
> PCIE clocks		ESC: Exit
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* This item appears only when enabling Port8xh Decode.

Feature	Option	Description
DMI Link ASPM Control	[Disabled], [L0s], [L1], [L0sL1], [Auto]	The control of Active State Power Management of the DMI Link.
Port8xh Decode	[Disabled], [Enabled]	PCI Express Port8xh Decode Enable / Disable.
Port8xh Decode Port#	Value input	Select PCI Express Port8xh Decode Root Port. User to ensure port availability
PCIe function swap	[Disabled], [Enabled]	When Disabled, prevents PCIE rootport function swap. If any function other than 0th is enabled, 0th will become visible.
PCH PCIE Clock Gating	[Disabled], [Enabled]	PCH PCI Express Clock Gating Enable / Disable for all port
PCH PCIE Power Gating	[Disabled], [Enabled]	PCH PCI Express Power Gating Enable / Disable for all port

Figure 82: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCIe EQ settings

Aptio Setup – AMI		
Chipset		
PCIe EQ override	[Disabled]	
PCIe EQ method*	[PCIe hardware EQ]	
PCIe EQ mode*	[Use presets during EQ]	
EQ PH1 downstream port transmitter present*	0	
EQ PH1 upstream port transmitter present*	0	
Enable EQ phase 2 local transmitter override*	[Disabled]	
Number of presents or coefficients used during phase 3*	0	

Aptio Setup – AMI		
Chipset		
Preset 0*(1)	0	
Preset 1*(1)	0	
Preset 2*(1)	0	
Preset 3*(1)	0	
Preset 4*(1)	0	
Preset 5*(1)	0	
Preset 6*(1)	0	
Preset 7*(1)	0	
Preset 8*(1)	0	
Preset 9*(1)	0	
Preset 10*(1)	0	
Pre-cursor coefficient 0*(2)	0	
Post-cursor coefficient 0*(2)	0	
Pre-cursor coefficient 1*(2)	0	
Post-cursor coefficient 1*(2)	0	
Pre-cursor coefficient 2*(2)	0	
Post-cursor coefficient 2*(2)	0	
Pre-cursor coefficient 3*(2)	0	
Post-cursor coefficient 3*(2)	0	
Pre-cursor coefficient 4*(2)	0	
Post-cursor coefficient 4*(2)	0	
Pre-cursor coefficient 5*(2)	0	
Post-cursor coefficient 5*(2)	0	→←: Select Screen
Pre-cursor coefficient 6*(2)	0	↑ ↓: Select Item
Post-cursor coefficient 6*(2)	0	Enter: Select
Pre-cursor coefficient 7*(2)	0	+/-: Change Opt.
Post-cursor coefficient 7*(2)	0	F1: General Help
Pre-cursor coefficient 8*(2)	0	F2: Previous Values
Post-cursor coefficient 8*(2)	0	F3: Optimized Defaults
Pre-cursor coefficient 9*(2)	0	F4: Save & Exit
Post-cursor coefficient 9*(2)	0	ESC: Exit
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* These items appear only when enabling PCIe EQ override.

(1) These items appear only when selecting Use presets during EQ for PCIe EQ mode.

(2) These items appear only when selecting Use coefficients during EQ for PCIe EQ mode.

Feature	Option	Description
PCIe EQ override	[Disabled], [Enabled]	Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process
PCIe EQ method	[PCIe hardware EQ], [PCIe fixed EQ]	Choose PCIe EQ method
PCIe EQ mode	[Use presets during	Choose EQ mode.

Feature	Option	Description
	EQ], [Use coefficients during EQ]	Preset mode – root port will use presets during EQ process, Coefficient mode – root port will use coefficients during EQ process
EQ PH1 downstream port transmitter preset	Value input	Choose the value of the preset that will be used during phase 1 of the equalization
EQ PH1 upstream port transmitter preset	Value input	Choose the value of the preset that will be used during phase 1 of the equalization
Enable EQ phase 2 local transmitter override	[Disabled], [Enabled]	EQ Phase 2 local transmitter override can be used to debug issues with PCI devices equalization.
Number of presets or coefficients used during phase 3	Value input	Select how many presets or coefficients will be used during phase 3 of EQ. Please not that you have to set all of the list entries to valid values. The interpretation of this field depends on PCIe EQ mode
Preset 0..10	Value input	Choose the target preset value
Pre-cursor coefficient 0..9	Value input	Choose the target pre-cursor coefficient value
Post-cursor coefficient 0..9	Value input	Choose the target post-cursor coefficient value

Figure 83: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCI Express Root Port 5 / 7 / 8 / 9 / 10 / 12

Aptio Setup – AMI		
Chipset		
PCI Express Root Port 5 / 7 / 8 / 9 / 10 / 12	[Enabled]	
Connection Type*	[Slot]	
ASPM*	[Auto]	
L1 Substates*	[L1.1 & L1.2]	
L1 Low*	[Enabled]	
ACS*	[Enabled]	
PTM*	[Enabled]	
DPC*	[Disabled]	
EDPC*	[Enabled]	
URR*	[Disabled]	
FER*	[Disabled]	
NFER*	[Disabled]	
CER*	[Disabled]	
SEFE*	[Disabled]	
SENFE*	[Disabled]	
SECE*	[Disabled]	
PME SCI*	[Enabled]	
Hot Plug*	[Disabled]	
Advanced Error Reporting*	[Enabled]	
PCIe Speed*	[Auto]	

Aptio Setup – AMI		
Chipset		
Transmitter Half Swing*	[Disabled]	
Detect Timeout*	0	
Extra Bus Reserved*	0	
Reserved Memory*	10	
Reserved I/O*	4	
PCH PCIe LTR Configuration*		
LTR*	[Enabled]	
Snoop Latency Override*#	[Auto]	→←: Select Screen
Snoop Latency Value*#(1)	60	↑ ↓: Select Item
Snoop Latency Multiplier*#(1)	[1024 ns]	Enter: Select
Non Snoop Latency Override*#	[Auto]	+/-: Change Opt.
Non Snoop Latency Value*#(2)	60	F1: General Help
Non Snoop Latency Multiplier*#(2)	[1024 ns]	F2: Previous Values
		F3: Optimized Defaults
LTR Lock*	[Disabled]	F4: Save & Exit
Peer Memory Write Enable*	[Disabled]	ESC: Exit
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* These items appear only when enabling PCI Express Root Port 5 / 7 / 8 / 9 / 10 / 12.

These items appear only when enabling LTR.

(1) These items appear only when selecting Manual for Snoop Latency Override.

(2) These items appear only when selecting Manual for Mon Snoop Latency Override.

Feature	Option	Description
PCI Express Root Port 5 / 7 / 8 / 9 / 10 / 12	[Disabled], [Enabled]	Control the PCI Express Root Port.
Connection Type	[Bulit-in], [Slot]	[Built-in]: a built-in device is connected to this rootport. SlotImplemented bit will be clear. [Slot]: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
ASPM	[Disabled], [L1], [Auto]	Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM
L1 Substates	[Disabled], [L1.1], [L1.1 & L1.2]	PCI Express L1 Substates settings.
L1 Low	[Disabled], [Enabled]	PCI Express L1 Low Substate Enable / Disable.
ACS	[Disabled], [Enabled]	Enable / Disable Access Control Services Extended Capability
PTM	[Disabled], [Enabled]	Enable / Disable Precision Time Measurement

Feature	Option	Description
DPC	[Disabled], [Enabled]	Enable / Disable Downstream Port Containment
EDPC	[Disabled], [Enabled]	Enable / Disable Rootport extensions for Downstream Port Containment
URR	[Disabled], [Enabled]	PCI Express Unsupported Request Reporting Enable / Disable.
FER	[Disabled], [Enabled]	PCI Express Device Fatal Error Reporting Enable / Disable.
NFER	[Disabled], [Enabled]	PCI Express Device Non-Fatal Error Reporting Enable / Disable.
CER	[Disabled], [Enabled]	PCI Express Device Correctable Error Reporting Enable / Disable.
SEFE	[Disabled], [Enabled]	Root PCI Express System Error on Fatal Error Enable / Disable.
SENFE	[Disabled], [Enabled]	Root PCI Express System Error on Non-Fatal Error Enable / Disable.
SECE	[Disabled], [Enabled]	Root PCI Express System Error on Correctable Error Enable / Disable.
PME SCI	[Disabled], [Enabled]	PCI Express PME SCI Enable / Disable.
Hot Plug	[Disabled], [Enabled]	PCI Express Hot Plug Enable / Disable.
Advanced Error Reporting	[Disabled], [Enabled]	Advanced Error Reporting Enable / Disable.
PCIe Speed	[Auto], [Gen1], [Gen2], [Gen3], [Gen4]	Configure PCIe Speed
Transmitter Half Swing	[Disabled], [Enabled]	Transmitter Half Swing Enable / Disable.
Detect Timeout	Value input	The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
Extra Bus Reserved	Value input	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	Value input	Reserved Memory for this Root Bridge (1-20) MB
Reserved I/O	Value input	Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
LTR	[Disabled], [Enabled]	PCH PCIE Latency Reporting Enable / Disable
Snoop Latency Override	[Disabled], [Manual], [Auto]	Snoop Latency Override for PCH PCIE. [Disabled]: Disable override. [Manual]: Manually enter override values. [Auto] (default): Maintain default BIOS flow.
Snoop Latency Value	Value input	LTR Snoop Latency value of PCH PCIE
Snoop Latency Multiplier	[1 ns], [32 ns],	LTR Snoop Latency Multiplier of PCH PCIE

Feature	Option	Description
	[1024 ns], [32768 ns], [1048576 ns], [33554432 ns]	
Non Snoop Latency Override	[Disabled], [Manual], [Auto]	Non Snoop Latency Override for PCH PCIE. [Disabled]: Disable override. [Manual]: Manually enter override values. [Auto] (default): Maintain default BIOS flow.
Non Snoop Latency Value	Value input	LTR Non Snoop Latency value of PCH PCIE
Non Snoop Latency Multiplier	[1 ns], [32 ns], [1024 ns], [32768 ns], [1048576 ns], [33554432 ns]	LTR Non Snoop Latency Multiplier of PCH PCIE
LTR Lock	[Disabled], [Enabled]	PCIE LTR Configuration Lock
Peer Memory Write Enable	[Disabled], [Enabled]	Peer Memory Write Enable / Disable

Figure 84: BIOS Chipset Setup Menu – PCH-IO Configuration – PCI Express Configuration – PCIE clocks

Aptio Setup – AMI		
Chipset		
Clock0 assignment	[Enabled]	
ClkReq for Clock0	[Platform-POR]	
Clock1 assignment	[Enabled]	
ClkReq for Clock1	[Platform-POR]	
Clock2 assignment	[Enabled]	
ClkReq for Clock2	[Platform-POR]	
Clock3 assignment	[Enabled]	
ClkReq for Clock3	[Platform-POR]	
Clock4 assignment	[Enabled]	
ClkReq for Clock4	[Platform-POR]	
Clock5 assignment	[Enabled]	
ClkReq for Clock5	[Platform-POR]	→←: Select Screen
Clock6 assignment	[Enabled]	↑ ↓: Select Item
ClkReq for Clock6	[Platform-POR]	Enter: Select
Clock7 assignment	[Enabled]	+/-: Change Opt.
ClkReq for Clock7	[Platform-POR]	F1: General Help
Clock8 assignment	[Enabled]	F2: Previous Values
ClkReq for Clock8	[Platform-POR]	F3: Optimized Defaults
Clock9 assignment	[Enabled]	F4: Save & Exit
ClkReq for Clock9	[Platform-POR]	ESC: Exit

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Chipset
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Feature	Option	Description
Clock0..9 assignment	[Platform-POR], [Enabled], [Disabled]	[Platform-POR]: clock is assigned to PCIe port or LAN according to board layout. [Enabled]: keep clock enabled even if unused. [Disabled]: Disable clock.
ClkReq for Clock0..9	[Platform-POR], [Disabled]	[Platform-POR]: CLKREQ signal is assigned to CLKSRC according to board layout. [Disabled]: CLKREQ will not be used.

Figure 85: BIOS Chipset Setup Menu — PCH-IO Configuration — SATA Configuration

Aptio Setup – AMI		
Chipset		
SATA Configuration		
SATA Controller(s)	[Enabled]	
SATA Mode Selection*	[AHCI]	
SATA Test Mode*	[Disabled]	
Aggressive LPM Support*(1)	[Enabled]	
Serial ATA Port 0*	Empty	
Software Preserve*	Unknown	
Port 0*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	
Mechanical Presence Switch*(2)	[Disabled]	
Spin Up Device*	[Disabled]	
SATA Device Type*	[Hard Disk Drive]	
Topology*	[Unknown]	
SATA Port 0 DevSlp*	[Disabled]	
DITO Configuration*	[Disabled]	
DITO Value*(4)	625	
DM Value*(4)	15	
Serial ATA Port 1*	Empty	
Software Preserve*	Unknown	
Port 1*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	
Mechanical Presence Switch*(2)	[Disabled]	

Aptio Setup – AMI		
Chipset		
Spin Up Device*	[Disabled]	
SATA Device Type*	[Hard Disk Drive]	
Topology*	[Unknown]	
SATA Port 1 DevSlp*	[Disabled]	
DITO Configuration*	[Disabled]	
DITO Value*(4)	625	
DM Value*(4)	15	
Serial ATA Port 2*	Empty	
Software Preserve*	Unknown	
Port 2*	[Enabled]	
Hot Plug*	[Disabled]	
Configured as eSATA*(3)	Hot Plug supported	
External*	[Disabled]	→←: Select Screen
Mechanical Presence Switch*(2)	[Disabled]	↑ ↓: Select Item
Spin Up Device*	[Disabled]	Enter: Select
SATA Device Type*	[Hard Disk Drive]	+/-: Change Opt.
Topology*	[Unknown]	F1: General Help
SATA Port 2 DevSlp*	[Disabled]	F2: Previous Values
DITO Configuration*	[Disabled]	F3: Optimized Defaults
DITO Value*(4)	625	F4: Save & Exit
DM Value*(4)	15	ESC: Exit
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* These items appear only when enabling SATA Controller(s).

(1) This item appears only when disabling SATA Test Mode.

(2) This item appears only when enabling Hot Plug.

(3) This item appears only when disabling External.

(4) These items appear only when enabling DITO Configuration.

Feature	Option	Description
SATA Controller(s)	[Enabled], [Disabled]	Enable / Disable SATA Device.
SATA Mode Selection	[AHCI]	Read only item
SATA Test Mode	[Enabled], [Disabled]	Test Mode Enable / Disable (Loop Back).
Aggressive LPM Support	[Disabled], [Enabled]	Enable PCH to aggressively enter link power state.
Port 0..2	[Disabled], [Enabled]	Enable or Disable SATA Port
Hot Plug	[Disabled], [Enabled]	Designates this port as Hot Pluggable.
External	[Disabled], [Enabled]	Marks this port as external.

Feature	Option	Description
Mechanical Presence Switch	[Disabled], [Enabled]	Controls reporting if this port has an Mechanical Presence Switch. Note: Requires hardware support.
Spin Up Device	[Disabled], [Enabled]	If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	[Hard Disk Drive], [Solid State Drive]	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
Topology	[Unknown], [ISATA], [Direct Connect], [Flex], [M2]	Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
SATA Port 0..2 DevSlp	[Disabled], [Enabled]	Enable / Disable SATA Port 0..2 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
DITO Configuration	[Disabled], [Enabled]	Enable / Disable DITO Configuration
DITO Value	Value input	DITO Value
DM Value	Value input	DM Value

Figure 86: BIOS Chipset Setup Menu – PCH-IO Configuration – USB Configuration

Aptio Setup – AMI		
Chipset		
USB Configuration		
xDCI Support	[Disabled]	
USB2 PHY Sus Well Power Gating	[Enabled]	
USB PDO Programming	[Enabled]	
USB Overcurrent	[Enabled]	
USB Overcurrent Lock	[Enabled]	
USB Audio Offload	[Enabled]	
Enable HSII on xHCI	[Enabled]	
USB3.1 Portx Speed Selection	0	
USB Port Disable Override	[Disabled]	
USB SW Device Mode Port #0*	[Disabled]	
USB SW Device Mode Port #1*	[Disabled]	
USB SW Device Mode Port #2*	[Disabled]	
USB SW Device Mode Port #3*	[Disabled]	
USB SW Device Mode Port #4*	[Disabled]	
USB SW Device Mode Port #5*	[Disabled]	

Aptio Setup – AMI		
Chipset		
USB SW Device Mode Port #6*	[Disabled]	
USB SW Device Mode Port #7*	[Disabled]	
USB SW Device Mode Port #8*	[Disabled]	
USB SW Device Mode Port #9*	[Disabled]	
USB SS Physical Connector #0*	[Enabled]	
USB SS Physical Connector #1*	[Enabled]	
USB SS Physical Connector #2*	[Enabled]	
USB SS Physical Connector #3*	[Enabled]	
USB HS Physical Connector #0*	[Enabled]	
USB HS Physical Connector #1*	[Enabled]	→ ←: Select Screen
USB HS Physical Connector #2*	[Enabled]	↑ ↓: Select Item
USB HS Physical Connector #3*	[Enabled]	Enter: Select
USB HS Physical Connector #4*	[Enabled]	+/-: Change Opt.
USB HS Physical Connector #5*	[Enabled]	F1: General Help
USB HS Physical Connector #6*	[Enabled]	F2: Previous Values
USB HS Physical Connector #7*	[Enabled]	F3: Optimized Defaults
USB HS Physical Connector #8*	[Disabled]	F4: Save & Exit
USB HS Physical Connector #9*	[Enabled]	ESC: Exit
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* These items appear only when selecting Select Per-Pin for USB Port Disable Override.

Feature	Option	Description
xDCI	[Disabled], [Enabled]	Enable / Disable xDCI (USB OTG Device).
USB2 PHY Sus Well Power Gating	[Disabled], [Enabled]	Select 'Enabled' to enable SUS Well PG for USB2 PHY. This option has no effect on PCH-H.
USB PDO Programming	[Disabled], [Enabled]	Select 'Enabled' if Port Disable Override functionality is used.
USB Overcurrent	[Disabled], [Enabled]	Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC does not work.
USB Overcurrent Lock	[Disabled], [Enabled]	Select 'Disabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping date
USB Audio Offload	[Disabled], [Enabled]	Enable / Disable USB Audio Offload functionality
Enable HSII on xHCI	[Disabled], [Enabled]	Enable / Disable HSII feature. It may lead to increased power consumption.
USB3.1 Portx Speed Selection	Value input	PortX Speed Selection: 0: All ports in Gen 2 speed (Default) 1: Gen 1 speed for port 1 only 2: Gen 1 speed for port 2 only 3: Gen 1 speed for port 1 and port 2 4: Gen 1 speed for port 3 only

Feature	Option	Description
		5: Gen 1 speed for port 1 and port 3 … so on 15: All ports 1 – 4 are limited to Gen 1
USB Port Disable Override	[Disabled], [Select Per-Pin]	Selectively Enable / Disable the corresponding USB port from reporting a Device Connection to the controller.
USB SW Device Mode Port #0..9	[Disabled], [Enabled]	Enable Connector Event for device subscription.
USB SS Physical Connector #0..3	[Disabled], [Enabled]	Enable / Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.
USB HS Physical Connector #0..9	[Disabled], [Enabled]	Enable / Disable this USB Physical Connector (physical port). Once disabled, any USB devices plug into the connector will not be detected by BIOS or OS.

8.2.4. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The 3.5"-SBC-RPL provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Figure 87: BIOS Security Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range:					
Minimum Length		3		→ ←: Select Screen	
Maximum length		20		↑ ↓: Select Item	
				Enter: Select	
Administrator Password				+/-: Change Opt.	
User Password				F1: General Help	
				F2: Previous Values	
> Secure Boot				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Description
Administrator Password	Set administrator password
User Password	Set user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

Figure 88: BIOS Security Setup Menu – Secure Boot

Aptio Setup – AMI		
Security		
System Mode	Setup	
Secure Boot	[Disabled]	→ ←: Select Screen
	Not Active	↑ ↓: Select Item
		Enter: Select
Secure Boot Mode	[Standard]	+/-: Change Opt.
> Restore Factory Keys*		F1: General Help
> Reset To Setup Mode*		F2: Previous Values
		F3: Optimized Defaults
> Key Management*		F4: Save & Exit
		ESC: Exit
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*These sub-screen links function only when selecting Custom for Secure Boot Mode.

Feature	Option	Description
Secure Boot	[Disabled], [Enabled]	Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.
Secure Boot Mode	[Standard], [Custom]	Secure Boot mode options: Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.
Restore Factory Keys	[Yes], [No]	Force System to User Mode. Install factory default Secure Boot key databases.
Reset To Setup Mode	[Yes], [No]	Delete all Secure Boot key databases from NVRAM

Figure 89: BIOS Security Setup Menu – Secure Boot – Key Management

Aptio Setup – AMI				
Security				
Vendor Keys	Valid			
Factory Key Provision	[Disabled]			
> Restore Factory Keys				
> Reset To Setup Mode				
> Enroll Efi Image				
> Export Secure Boot variables				→ ←: Select Screen
				↑ ↓: Select Item
Secure Boot variable	Size	Keys	Key Source	Enter: Select
> Platform Key (PK)	0	0	No Keys	+/-: Change Opt.
> Key Exchange Keys (KEK)	0	0	No Keys	F1: General Help
> Authorized Signatures (db)	0	0	No Keys	F2: Previous Values
> Forbidden Signatures (dbx)	0	0	No Keys	F3: Optimized Defaults
> Authorized TimeStamps (dbt)	0	0	No Keys	F4: Save & Exit
> OsRecovery Signatures (dbr)	0	0	No Keys	ESC: Exit
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Feature	Option	Description
Factory Key Provision	[Disabled], [Enabled]	Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.
Reset Factory Keys	[Yes], [No]	Force System to User Mode. Install factory default Secure Boot key databases.
Reset to Setup Mode	[Yes], [No]	Delete all Secure Boot key databases from NVRAM.
Enroll Efi Image	Select a File system	Allow Efi image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).
Export Secure Boot variables	Select a File system	Save NVRAM content of Secure Boot variables to a file
Platform Key (PK)	[Details], [Export], [Update], [Delete]	Enroll Factory Defaults or load certificates from a file: 1. Public Key Certificate: (a) EFI_SIGNATURE_LIST (b) EFI_CERT_X509 (DER) (c) EFI_CERT_RSA2048 (bin) (d) EFI_CERT_SHAXXX 2. Authenticated UEFI Variable 3. EFI PE / COFF Image (SHA256) Key Source: Factory, Modified, Mixed
Key Exchange Keys (KEK)	[Details], [Export], [Update], [Append], [Delete]	
Authorized Signatures (db)	[Details], [Export], [Update], [Append],	

Feature	Option	Description
	[Delete]	
Forbidden Signatures (dbx)	[Details], [Export], [Update], [Append], [Delete]	
Authorized TimeStamps (dbt)	[Update], [Append]	
OsRecovery Signatures (dbr)	[Update], [Append]	

8.2.4.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not known, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

8.2.5. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 90: BIOS Boot Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Boot Configuration					
Setup Prompt Timeout		1			
Bootup NumLock State		[Off]		→←: Select Screen	
Quiet Boot		[Disabled]		↑ ↓: Select Item	
				Enter: Select	
Boot Option Priorities				+/-: Change Opt.	
Boot Option #1		[UEFI: Built-in EFI Shell]		F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Setup Prompt Timeout	Value Input	Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
Bootup NumLock State	[On], [Off]	Select the keyboard NumLock state [On]: The keys on the keypad will act as numeric keys. [Off]: The keys on the keypad will act as cursor keys.
Quiet Boot	[Disabled], [Enabled]	Enables or disables Quiet Boot option
Boot Option #1	[UEFI: Built-in EFI Shell], [Disabled]	Sets the system boot order

8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 91: BIOS Save & Exit Setup Menu

Aptio Setup – AMI					
Main	Advanced	Chipset	Security	Boot	Save & Exit
Save Options					
Save Changes and Exit					
Discard Changes and Exit					
Save Changes and Reset					
Discard Changes and Reset					
Save Changes					
Discard Changes				→ ←: Select Screen	
				↑ ↓: Select Item	
Default Options				Enter: Select	
Restore Defaults				+/-: Change Opt.	
Save as User Defaults				F1: General Help	
Restore User Defaults				F2: Previous Values	
				F3: Optimized Defaults	
Boot Override				F4: Save & Exit	
UEFI: Built-in EFI Shell*				ESC: Exit	
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* This item appears only when selecting UEFI: Built-in EFI Shell for Boot Option #1 in Boot Setup Menu.

Feature	Description
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset system setup without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.
Restore Defaults	Restore / Load Default values for all the setup options.
Save as User Defaults	Save the changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.
UEFI: Built-in EFI Shell	This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order. If booting to EFI Shell this way, an exit from the shell returns to Setup.

Appendix A: List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 53: List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AT	Advanced Technology
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input / Output System
BSP	Board Support Package
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDC	Display Data Channel
DIO	Digital Input / Output
DP	DisplayPort
ECC	Error-Correcting Code
EEE	Electrical and Electronic Equipment
EOS	Electrical OverStress
ESD	ElectroStatic Discharge
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Device
LVDS	Low-Voltage Differential Signaling
ME F/W	Management Engine Firmware
mPCIe	mini Peripheral Component Interconnect express
NGFF	Next Generation Form Factor
PC-AT	Personal Computer - Advanced Technology
PCB	Printed Circuit Board
PSU	Power Supply Unit
PVC	PolyViny Chloride
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital memory card
SDP	Serial Download Protocol
SELV	Safety Extra-Low Voltage
SIM	Subscriber Identity Module
SMBus	System Management Bus
SoC	System on Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
TDP	Thermal Design Power
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
UTP	Update Transfer Protocol
VGA	Video Graphics Array
WDT	WatchDog Timer
WEEE	Waste Electrical and Electronic Equipment

About Kontron

Kontron is a global leader in IoT / Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

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